Application

2015-03-31

Vetenskapsrådet

2015-03960	Björkman, Mårten	NT-2

Information about applicant

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Project site: CVAP, Datorseende och robotik

Information about application

Call name: Forskningsbidrag Stora utlysningen 2015 (Naturvetenskap och teknikvetenskap)

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Project title (english): Neuromorphic architectures for sensorimotor couplings on robots

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Keywords: cognitive systems, sensorimotor couplings, deep networks, neuromorphic architectures, robotic manipulation

Funds applied for

Year:	2016	2017	2018	2019
Amount:	1,382,000	1,467,000	1,561,000	1,660,000

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Descriptive data

Project info

Project title (Swedish)*

Neuromorfiska arkitekturer för sensorimotoriska kopplingar på robotar

Project title (English)*

Neuromorphic architectures for sensorimotor couplings on robots

Abstract (English)*

For an autonomous robot to acquire cognitive skills comparable to those of humans, it needs to learn to predict the consequences of its own actions and apply these predictions to solve tasks that are placed on it. In this project we will let a humanoid robot explore its embodiment and learn such sensorimotor couplings on its own, rather than assuming a human designer to provide information on the robot and the world it is residing in by careful modelling. The immediate benefit is that the designer is relieved from the heavy burden of off-line sensory and kinematic calibration. It would also make the system more robust, when changes due to wear-and-tear can be adjusted for through adaptation, instead of stopping the robot for it be re-calibrated.

Our target application is the problem of object reaching and grasping, a task that is complex in the sense that it involves large amounts of multimodal sensory data that need to be processed and interpreted. The task will be used to illustrate the benefits of a tighter coupling between perception and action during sensorimotor learning, and test the feasibility of deep neural networks as a general fabric for representing such couplings. It further serves as a means to test the way humans are believed to acquire sensorimotor skills, by replicating the behaviour on a humanoid robot, making the robot self-learn object grasping through a sequence of skills of gradually increasing complexity.

In earlier research we used in particular Gaussian processes to learn sensorimotor couplings, which is possible as long as long as the dimensionality of sensory data is limited. However, to directly learn sensorimotor couplings from raw high-dimensional sensory data, such as visual and tactile data, we will adopt deep networks to learn action relevant sensory features and use these to represent complete sensorimotor couplings in the same learning framework. We do this to benefit from the same generative and discriminative power of such networks in robotics, as has previously been observed in image classification and natural language processing. However, despite being flexible and effective tools for learning, there is a high computational cost associated with learning of deep networks.

To cope with the low power requirements of autonomous robots, combined with the need for online learning, we will exploit the fact that the regular structure of deep networks allows for massive parallelism and develop a dedicated Dynamically Reconfigurable Neuromorphic Fabric (DRNF) for implementation of deep networks on silicon. This will be done by simultaneously developing algorithms for sensorimotor modelling and let the algorithms set the requirements of the developed fabric. The fabric will contain reconfigurable computational cells, with DRAM organised in tiles stacked in 3D above the computational die. Elastic partitions of cells and tiles, interconnected through a 3D Network on Chip, will introduce flexibility in the way parallelism at different levels of the neural network can be exploited. With the combination of 3D stacking and elastic partitions we will reach the memory capacity and computational power required for online learning of deep networks for real-time operation on robots.

The work will be conducted as two inter-related work packages running in parallel, one for sensorimotor modelling and one for the neuromorphic implementation. Two candidates will be deployed for the project, a doctoral student and a postdoctoral one, the latter of which already has funding from KTH. The two will be supervised by the applicants and other faculty members. While algorithms will developed as a sequence of acquired skills, starting with object detection and tracking (month 12), then reaching while avoiding obstacles (month 30), to end with grasp contact point and configuration search (month 48), the hardware will be developed in a sequence with four milestones from specification and dimensioning to implementation and final verification.

Popular scientific description (Swedish)*

För att en självgående robotik ska kunna utveckla kognitiva färdigheter jämförbara med en människas, måste roboten själv lära sig förstå de möjligheter och begränsningar som dess kropp medger. Roboten måste förstå kopplingen mellan de aktioner den utför på den omgivning den befinner sig i och de förändringar i sinneintryck som kommer som ett resultat av denna påverkan. Dessa sensorimotoriska kopplingar måste med en dator representeras på ett sådant sätt att roboten lätt kan göra prediktioner av vilka resultat som kan förväntas om den utför en viss aktion, detta för att kunna planera en längre sekvens av aktioner för att lösa ett mer komplext problem problem, såsom att hitta ett borttappat objekt för att därefter plocka upp det. Representationen måste vara så rik och flexibel att alla variationer av aktioner och sinnesuttryck kan beskrivas, men inte så komplex att den inte kan utnyttjas och läras i real-tid, alltså snabbt nog i relation till robotens egen rörelse. I denna studie avser vi att använda oss av djupa neurala nätverk för att representera sensorimotoriska kopplingar, eftersom sådana nätverk på senare år visat sig kraftfulla nog att lösa större problem inom bildigenkänning, ljud- och språk-tolkning, problem som mer traditionella metoder haft svårt att hantera på ett effektivt sätt. Förhoppningen är att dra nytta av samma goda egenskaper för tillämpningar inom robotik och få en robot att, utan något som helst stöd från en människa, först lära sig hantera sin kropp för att därefter kunna plocka upp objekt den observerar i sin närmiljö.

I tidigare studier av sensorimotoriska kopplingar på robotar har man oftast infört begränsningar i vilka typer av aktioner och sinnesintryck som ansetts möjliga, ibland genom att helt sonika skapa insektsliknande robotar vars sinnessystem är mycket enklare än en människas. Om målet är att studera sensorimotoriska kopplingar som sådana må detta vara acceptabelt, men om man med tiden vill nå människoliknande kognition bör man undvika alla sådana medvetna begränsningar. En svårighet med djupa neurala nätverk är dock den beräkningskraft och stora mängd minne som krävs, och det faktum att självgående robotar måste vara strömsnåla för att att kunna vara aktiva under en längre tid. En lösning är att koppla roboten via ett trådlöst nätverk till en superdator där beräkningarna görs. Detta begränsar dock roboten till en laboratoriemiljö, utan att någonsin kunna röra sig i en verklig miljö. I detta projekt avser vi inte bara att utveckla metoder för inlärning av sensorimotoriska kopplingar på robotar med hjälp av djupa neurala nätverk och tillämpa dessa kopplingar i praktiken, utan också utveckla ett neuromorfiskt chip (neurala nätverk på kisel) speciellt för ändamålet. Tanken är att, för att nå bästa möjliga lösning, låta utveckling av algoritmer och en anpassad hårdvara gå hand i hand, eftersom båda dessa komponenter påverkar varandra.

Ett viktigt skäl till varför neuromorfiska chip är av intresse är den minnesbarriär som begränsat vidareutvecklingen av vanliga datorer. Eftersom minnet i en typisk dator är skilt från beräkningskärnan, har det ingen betydelse om beräkningarna kan göras snabbare, om inte åtkomsten till minnet förbättras i motsvarande utsträckning. I fallet med djupa neurala nätverk, så är denna effekt högst påtaglig, eftersom seende och andra sinnen genererar en strid ström data som måste bearbetas för att tolkas. I neuromorforiska chip försöker man komma runt minnesbarriären genom att ha många parallellt arbetande beräkningskärnor med minne placerat så nära kärnorna som möjligt. I vårt fall avser vi att placera minnet i flera lager rakt ovanpå chipytan där beräkningar görs. Flera kärnor som är tänkta att göra samma slags beräkningar, men på olika data, kan sedan konfigureras i elastiska uppdelningar med snabb strömmad åtkomst till minnet. På så sätt kan vi både bidraga till forskningen inom nästa generations datorer, samtidigt som vi kan utveckla kraftfullare representationer av sensorimotoriska kopplingar än vad som tidigare varit möjligt.

Project period

Number of project years*

4

Calculated project time*

2016-01-01 - 2019-12-31

Classifications

Select a minimum of one and a maximum of three SCB-codes in order of priority.

Select the SCB-code in three levels and then click the lower plus-button to save your selection.

SCB-codes*	1. Naturvetenskap > 102. Data- och informationsvetenskap (Datateknik) > 10207. Datorseende och robotik (autonoma system) 1. Naturvetenskap > 102. Data- och informationsvetenskap (Datateknik) > 10206. Datorteknik

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Enter a minimum of three, and up to five, short keywords that describe your project.

Keyword 1*

cognitive systems

Keyword 2*

sensorimotor couplings

Keyword 3*

deep networks

Keyword 4

neuromorphic architectures

Keyword 5

robotic manipulation

Ethical considerations

Specify any ethical issues that the project (or equivalent) raises, and describe how they will be addressed in your research. Also indicate the specific considerations that might be relevant to your application.

Reporting of ethical considerations*

There are no ethical consideration required for the proposed problem.

The project includes handling of personal data

No

The project includes animal experiments

No

Account of experiments on humans

No

Research plan

Neuromorphic architectures for sensorimotor couplings on robots

1 Purpose and Aims

With biological systems seen as proofs of existence, biology has long served as an inspiration for the design of robotic systems. In developmental robotics the goal is to reach human-level cognitive abilities by letting a robot learn from continuous interaction with the environment it is residing in[1]. Inspiration is found from observations of Piaget[2] that humans develop sensorimotor and other skills in stages, where one stage is a prerequisite for the next, leading to gradually more complex skills obtained. Developmental robotics represents a shift away from traditional robotics, where the human designer played a central role in defining task-specific representations and motor schemas[3]. Instead the robot is assumed to learn its own sensorimotor capabilities, while continuously interacting with its environment[4]. Emphasis is placed on the tight coupling between perception and action, with less focus on planning and representation that used to be the case in traditional robotics[5].

In this project we will use biologically inspired deep neural networks to represent sensorimotor couplings and let the sensory and motoric capacities of a robot directly drive the representation, with minimal interference from a human designer. This relieves the robot designer from the burden of carefully performing off-line sensory and kinematic calibration of the system. Through adaptation it also allows the robot to overcome changes in its dynamics due to wear-and-tear or complete malfunctions in some of its parts. Finally, through self-learning the robot only learns what is relevant given the limitations of its own embodiment, while redundant information is effectively discarded and never represented.

We will focus on robotic reaching and grasping[6], a task that is complex in the sense that it requires a robot to first understand its own embodiment and then combine massive amount of information from various sensory modalities to control its motor system. Besides applying deep networks for developmental robotics, we will also study their implementation aspects by designing a neuromorphic fabric for representing such networks on silicon. Thus with respect to Marr's three levels at which any machine carrying out an information-processing task must be understood[7], we will explore two levels, the algorithmic and the implementation levels. The reason for doing so is the strong inter-dependence between the two levels and the fact that a high processing speed at a low power budget is required for robotic applications.

Our motivation for using deep networks comes from recent studies where such networks show superior performance in challenging image classification benchmarks that have earlier been dominated by less biologically motivated machine learning techniques. Deep networks provide advantages compared to networks with only one or two layers[8]. First, they support feature re-use from different levels of the hierarchy, where the number of ways features can be combined increases exponentially with depth. This opens up the possibility for multiple robotic behaviours to be represented by the same deep network. Second, multiple layers lead to a gradual decrease in abstraction of incoming sensory data and can be trained to capture

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[7] Marr, D., "Vision: A Computational Approach", San Francisco, Freeman & Co, 1982.
[8] Bengio, Y., Courville, A., & Vincent, P., "Representation Learning: A Review and New Perspectives", IEEE Trans. on Pattern Analysis and Machine Intelligence, 2013.

invariances relevant for individual behaviours. This is in contrast to typical computer vision systems that often contain a single (hand-crafted) feature detection layer and another layer trained for a particular task, something that is true also for robotics.

In the project we will also develop a custom hardware implementation for deep network based sensorimotor modelling. The design will have near ASIC like efficiency by customising the computation, storage and interconnect hierarchy. However, to enable experimentation and use of different network structures, algorithms and problem dimensions, we will adopt a coarse grain reconfiguration strategy to amortize engineering and manufacturing cost. The design will be a tiled parallel distributed architecture that matches very well the nature of deep networks and significantly reduces the cost of design and verification, as the key effort is in dimensioning the fabric and designing a single tile and replicating it. We plan to use 3D stacked DRAM dies to address the bottleneck of memory bandwidth for higher performance, and make the design more scalable. Though exact dimensioning of the requirements will be carried out in the first year of the project, our preliminary best-effort estimate is that the hardware would need to deliver 100s of GFLOPs and would need a few GBs of storage.

The project can be summarized in three challenges. The **first challenge** is to make a robot self-learn sensorimotor couplings that allow the robot to perform a task as complex as object grasping, while assuming no prior calibration or heuristics provided by a human designer. The **second challenge** is to adopt deep networks as a general framework for multimodal learning and show that these are equally applicable for motor control, as they have already shown to be for image classification, speech and language processing. Finally, the **third challenge** is to design a custom reconfigurable hardware implementation that provides real-time learning of sensorimotor couplings for robotic systems with a power envelope as low as 10 watts.

2 Survey of the field and progress beyond the state of the art

Computational modelling of vision has found inspiration from in particular Hubel & Wiesel, who suggested the visual cortex to be organized hierarchically with two types of alternating cells. Simple cells are responsive to different orientations in local receptive fields, whereas complex cells apply pooling, making responses more and more spatially invariant at higher levels of the hierarchy. The first computational model based on these observations is the Neocognitron[9], a model that used unsupervised learning for the simple cells and a final linear classifier on the output layer that was learned supervised. Since then a number of similar models have been proposed, such as Convolutional Networks (CNN)[10], HMAX[11] and Deep Belief Networks (DBN)[12], which are collectively referred to as deep networks.

2.1 Deep networks for sensorimotor learning on robots

Deep networks have shown to be competitive to state-of-the-art classification methods in computer vision. On the most demanding object classification benchmark currently available, all best performing methods to date are based on CNN[13]. Since the same networks trained for one classification task have shown to be successful also on novel tasks, deep networks have been proposed as general frameworks for visual processing[14]. Biology suggests that, at least

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[14] Donahue, J., Jia, Y., Vinyals, O., Hoffman, J., Zhang, N., Tzeng, E., Darrell, T., ”DeCAF: A Deep Convolutional Activation Feature for Generic Visual Recognition”, arXiv: 1310.1531, 2014.

for the lowest layers of the hierarchies, this might be true also for motoric tasks, such as reaching and grasping an object[15]. Another reason why deep networks are of interest for robotic systems is their proven ability to integrate sensory data from multiple modalities[16].

The use of deep networks for real-time robotic applications has so far been quite limited though, even if more shallow networks have existed for many years. Typically, deep networks are used for classification purposes, with vision seen as a support system, rather than being fully integrated with the motor system. There are examples of systems for robotic navigation that use CNNs for terrain classification[17] or for detection of suitable grasping positions on objects[18]. An example where complete sensorimotor relations are in fact learned using a deep network is a system for off-road robot navigation, where the network directly controls the steering angle[19]. However, supervised learning is done off-line using a large set of samples with angles that a human would use, not a result of exploration by the robot itself.

In robotics there has in recent years been a shift away from analytical methods that rely on precise modelling to more data-driven approaches for which relations are learned directly from the raw data, which is especially true for object grasping[20]. Despite this transition a typical learning process is still typically divided into two steps that are learned separately, feature learning and policy learning for action selection. The complexity of some sensory data, such as high-dimensional and diverse visual and tactile data, makes it difficult to learn full sensorimotor relations in an integrated framework. Different strategies have been used to cope with this, such as simply reducing the dimensionality of input data through subsampling. It is also possible to pre-process the data in a way that is known to suit the task, such as extracting object-specific features when learning affordances of objects[21],[22], where the human designer is the one deciding what features to extract, not a network that learns the relevant features on its own. Another possibility is to limit the study on sensorimotor relations to robots with sensory systems of lower complexity[23]. However, if the goal is to eventually reach human-like cognition, one should refrain from dimensionality reductions that cannot be motivated by redundancies with respect to embodiment of the robot.

Progress beyond the state-of-the-art*: To fully exploit the richness of in particular visual and tactile data and still be able to learn complete sensorimotor relations in a data-driven manner, we will in NEUROACT explore deep networks as a fabric for multimodal learning. The goal is to let a robot autonomously acquire sensorimotor skills while interacting with the environment, with as little prior information as possible required by a human designer. The benefit of this should not be understated. The need for recalibration of robotic systems is a constant obstacle for robot developers who aim for robustness during long-term operation,*

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often preventing such systems from eventually reaching a market place. With self-learning a robot can adapt to changes in its embodiment due to wear-and-tear and to changes in its working environment, making robots autonomous not just in name, but also in practice.

The three tasks described in section 3.1 will be used as demonstrators, illustrating the benefits of a tighter coupling between perception and action during sensorimotor learning, letting a robot learn to first detect an object, then reach towards the object while avoiding obstacles and finally grasp it. In a broader context, the three incremental tasks will serve as a means to test Piaget's theory on sensorimotor development[2]*, by replicating the way humans are believed to acquire sensorimotor skills on a humanoid robot.*

2.2 Accelerating deep networks

Numerous attempts have already been made to speed up deep networks by applying readily available parallel implementation platforms like GPUs, FPGAs, Coarse Grain Reconfigurable Architectures and ASICs. Scherer et al.[24] have shown the use of GPUs for accelerating CNNs. Their principle objective was to speed up the training of CNNs for high-resolution natural images. Such a task would take weeks on traditional CPUs and they report a speed up of two orders of magnitude. Ciresan et al.[25] also report use of GPUs for accelerating the training of large CNNs that take days instead of months on traditional CPUs.

Chakradhar et al.[26] have presented a novel dynamically reconfigurable architecture for CNN on a Xilinx FPGA and compared their results to Xeon processors and GPUs. Their key innovation is to differentiate the type of parallelism in different network layers and workload, and adjust the parallelism accordingly to best utilize the architecture, which is enabled by dynamic reconfiguration. They achieve 25-30 fps image recognition in various applications. Their solution outperforms a Xeon processor and a 128-core GPU by 4-9 times depending on application. Farabet et al.[27] have shown a runtime reconfigurable dataflow processor called NeuFlow, with an architecture organized as a 2D grid of customised coarse grain processing tiles with a smart memory access to off-chip memory. This design clearly shows an order of magnitude improvement compared to GPU when implemented in FPGA and two orders of magnitude improvement when implemented in 45nm IBM technology. Esmaeilzadeh et al.[28] have presented an ASIC based accelerator to efficiently speed up approximate programs with neural networks and showed a speedup of 2.3x and energy savings of 3.0x on average, with quality loss of at most 9.6%. Recently, Chen et al.[29] presented a hardware accelerator with special emphasis on memory efficiency. The proposed chip was 117.87x faster and promised an energy reduction of up to 21.08x, compared to a 128-bit 2GHz SIMD processor.

Progress beyond the state-of-the-art: *The hardware accelerated implementations for deep networks reviewed above, while providing promising speed, fall short of the objectives of NEUROACT on several counts. The FPGA and ASIC implementations do not deal with training, and while those on GPU do show substantial speed up in training, from weeks to hours, they are still not suitable for online learning on the targeted power budget of less than*

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[26] Chakradhar, S., Sankaradas, M., Jakkula, V., & Cadambi, S., "A dynamically configurable coprocessor for convolutional neural networks", ACM SIGARCH Computer Architecture News, vol. 38, no. 3, 2010.

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10 watts. Further, none of the state-of-the-art hardware implementations target the objective of sensorimotor modelling on robots, but image classification as the only application.

Our preliminary dimensioning of hardware to meet the algorithmic requirements clearly points to the non-scalability of existing approaches. They have two fundamental limitations: 1) they attempt parallelization of computation, without matching parallelization of memory access and 2) the storage architecture is off-chip worsening the memory access bottleneck and energy efficiency as storage demands increase. In contrast, the DRNF fabric that we propose later in section 3.2 not only uses a custom hardware architecture to improve the computational efficiency, it parallelizes both computation and storage access creating a more balanced and scalable architecture. By using 3D stacking for memory, we also propose an increase in memory capacity that will scale with memory access bandwidth. Finally, the ability to dynamically create elastic partitions with agility will provide versatility in deploying as much parallelism as the dimension of the DRNF fabric provide and desired by the algorithm and performance requirements

2.3 Preliminary Work

At Centre of Autonomous Systems (CAS), KTH, relations between perception and action, in the context of in particular object manipulation, have been studied for many years, with an early focus on developing seeing systems. These systems have over years become more complex and today include many of the processes found in biological seeing systems, processes such as visual attention, perceptual grouping and object recognition[30]. Numerous recent studies at CAS have included information from other sensory modalities than vision, e.g. haptic and proprioceptive information[31]. These studies have dealt with reasoning about objects through robotic manipulation in terms of the actions they afford[32] and applying actions to resolve ambiguities in the perceptual data[33]. Sensorimotor modelling has in most cases been done with Gaussian processes[34], but to improve the generative and discriminative power of models more recent studies have also included deep networks for tactile data[35], as well as for image classification[36]. More recent work on autonomous sensorimotor learning for hand-eye coordination is directly related to the project proposed here[37],[38]. The main applicant won the IROS Best Cognitive Paper Award in 2011 and was a finalist in 2013, for work on sensorimotor modelling for object manipulation.

The group at the Department of Electronic Systems, KTH, has been developing domain specific massively parallel coarse grain reconfigurable architectures. Two such architectures have so far been developed. Dynamically Reconfigurable Resource Array (DRRA)[39] targets Digital Signal Processing Applications. DRRA has been used by Huawei for a multi-mode

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[34] Rasmussen, C.E., "Gaussian processes for machine learning", 2006.

[35] Madry, M., Bo, L. Kragic, D., Fox, D., "ST-HMP: Unsupervised Spatio-Temporal Feature Learning for Tactile Data", in Proc. IEEE Int. Conf. on Robotics and Automation, June 2014.

[36] Razavian, A.S., Azizpour, H., Sullivan, J., Carlsson, S., "CNN Features off-the-shelf: an Astounding Baseline for Recognition", IEEE Conf. on Computer Vision and Pattern Recognition Workshops (CVPRW), 2014.

[37] A Ghadirzadeh, G Kootstra, A Maki, M Björkman, "Learning visual forward models to compensate for self-induced image motion", IEEE Conf. On Robot and Human Interactive Communication (RO-MAN), 2014.

[38] A Ghadirzadeh, A Maki, M Björkman, "A sensorimotor approach for self-learning of hand-eye coordination", IEEE/RSJ Int. Conf. on Intelligent Robots and Systems (IROS), 2015 (submitted).

[39] Shami, M.A., "Dynamically Reconfigurable Resource Array", PhD Thesis, Dept. of Electronic Systems, School of ICT, KTH. 2012. ISBN 978-91-7501-473-9. http://web.it.kth.se/~hemani/Athesis15.pdf

accelerator for their base stations and we have shown that the customisation enables us to come significantly closer to the hardwired solution in ASIC. This work got the HiPEAC Technology Transfer Award in 2012 and the PhD thesis was nominated for best PhD thesis. A parallel distributed memory fabric called DiMARCH[40] has been developed as a complement to DRRA. Another coarse grain reconfigurable fabric called BiCOM[41] for Bioinformatics Computer has also been developed that targets sequence alignment and phylogenetics applications. BiCOM has been comprehensively evaluated against GPUs and FPGAs and shows that on average it is two orders of magnitude superior to GPUs and an order of magnitude superior to FPGAs in computational efficiency. The group has considerable experience in developing custom high-level programming/compiler tools; Prof. Hemani's PhD thesis on high-level synthesis was commercialized by CADENCE. At present there are two PhD theses dedicated to developing libraries and compilers for the DRRA.

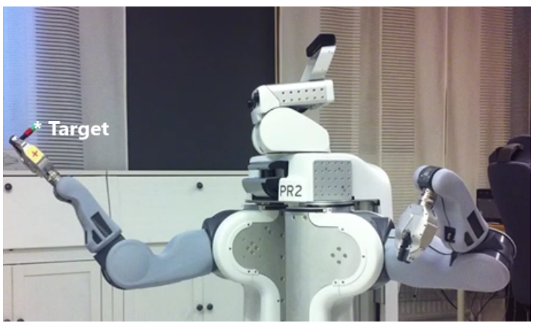
3 Project description

The goal of NEUROACT is to identify deep neural network structures for representation of sensorimotor relations on robotic systems and to design a neuromorphic architecture suitable for implementation of these structures on silicon. Our intention is to study these components in parallel to minimize potential mismatches between algorithms and architectures, and reach the highest possible processing speed given a limited power budget. The work will be carried out in two separate, but inter-dependent, work packages. Results obtained from algorithms developed in WP1 (section 3.1) are used for dimensioning the hardware in WP2 (section 3.2), which includes test series from real-world experiments, for simulation and verification.

3.1 Work Package 1: Deep network based object grasping

In earlier work we studied the problem of letting a humanoid robot autonomously learn how to perform hand-eye coordination[38]. The goal was to let the robot explore its embodiment and learn how to move its right hand towards an observed target point (see Figure 1). Hand-eye coordination was solved by successively learning two subtasks, fixation and reaching, each controlled by a Gaussian process based forward model. These models were continuously updated to predict the effect due to changes in joint positions and summarize the experience gained so far while executing the tasks. With no knowledge of the kinematic system given, other than the number of controllable joints and a set of predefined limits on these joint, we demonstrated how hand-eye coordination could be learned in a matter of minutes.

To this system we will add additional stages to the development of sensorimotor skills, in order for the robot to learn to also detect objects, reach towards these objects while avoiding obstacles, and finally grasp the objects. The work will be based on combinations of forward



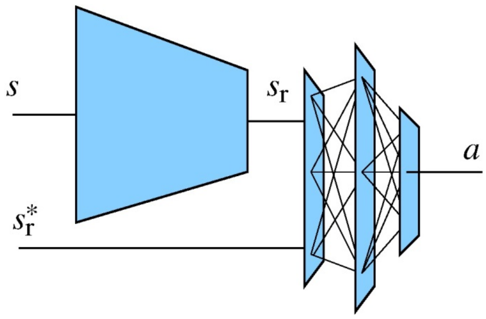


Figure 1 A humanoid learning reaching (left) and an inverse model for motor control (right). Sensory data s is abstracted to a state s_r through a deep network and combined with a target s_r^* to produce an action a, using either a Gaussian process model or another neural network.

[40] Tajammul, M.A., Shami, M.A., Hemani, A., "Segmented Bus Based Path Setup Scheme for a Distributed Memory Architecture", in Proc. IEEE Int. Symposium on Embedded Multicore Socs, Japan. pp 67-74, 2012.
[41] Liu, P. Ebrahim, F.O., Hemani, A., Paul, K., "A Coarse-Grained Reconfigurable Processor for Sequencing and Phylogenetic Algorithms in Bioinformatics", in Proc. Int. Conf. on Reconfigurable Computing and FPGAs, 2011

and inverse models[42]. While forward models are used to predict the effect of actions applied, inverse models include a control mechanism that given the current state results in an action to reach a particular target state, illustrated in Figure 1. This integration of perception and action will be done using either neural networks or Gaussian processes. However, to allow for high-dimensional sensory data, such as visual data, we will abstract the data with the help of deep networks that are learned with errors propagated back through the whole system, also through Gaussian process based models. By doing so only sensory features that are relevant to the end task are eventually learned. In terms of computational load this is the most critical part of the whole system, which is the motivation for developing dedicated hardware to increase speed, while keeping the power consumption low.

3.1.1 Task 1: Deep network based object detection and tracking (month 12)

We will adopt CNNs for object detection[45],[46] and apply these to the reaching scenario of our earlier work on humanoid robots, using the outputs of a deep network as states for the existing forward and inverse models. The network will be adapted for online learning of new object classes by retraining only the last hierarchical layers, while keeping lower layers for feature extraction intact. Earlier work at CAS has indicated that deep networks can be reused to new settings by only retraining the last layers and it is our belief that is the case also in this scenario[36]. To test whether this is in fact true, we will compare the results to the case of retraining of all layers.

A real-time system for object detection and tracking will be implemented on a GPU by exploiting temporal consistency. When nothing is known about the existence of an object, the full image will be considered for object detection. However, as soon as an object is detected, the system shall shift to object tracking, increasing the rate of continuous detection from 1 Hz to 20 Hz, by gradually shrinking the image window considered for detection, as long as the certainty in object position increases. The implemented system will be studied in a real world setting with household objects approached for interaction with the robotic arm, either in real-time or simulated real-time. Conclusions drawn on computational requirements and suitable deep network configurations will be used in WP2 (milestone M1) for dimensioning and early design commitments.

3.1.2 Task 2: Reinforcement learning for reaching with obstacle avoidance (month 30)

Sticking to the ambition of letting the robot acquire new skills through self-exploration alone, we will next study the problem of obstacle avoidance during reaching. A policy to control the arm will be learned through reinforcement learning with transition and reward functions modelled as Gaussian processes, similarly to our earlier work on disambiguation of objects through pushing[49]. For this task, however, a state space will be learned directly from the visual data, which was not the case in our earlier work.

By randomly moving the robotic arm around, a relation between the robot's view of its own arm and the corresponding joint positions will be learned with a deep auto-encoders[50], which serves as an abstraction of the visual data. Image data will thus be represented as a state in an embedded space with a dimensionality given by the number of joints of the arm. With the transition and reward functions expressed in the same embedded state space, where the

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[42] Jordan, M.I., Rumelhart, D.E., "Forward models: Supervised learning with a distal teacher", Cognitive science, vol. 16, no. 3, 307-354, 1992.
[45] R. Girshick, J. Donahue, T. Darrell, J. Malik, "Rich Feature Hierarchies for Accurate Object Detection and Semantic Segmentation", IEEE Conf. on Computer Vision and Pattern Recognition (CVPR), 2014.
[46] P. Sermanet, D. Eigen, X. Zhang, M. Mathieu, R. Fergus, Y. LeCun, "OverFeat: Integrated Recognition, Localization and Detection using Convolutional Networks", Int. Conf. on Learning Representations, 2014.
[49] Björkman, M., Bekiroglu, Y., Kragic, D., "Learning to Disambiguate Object Hypotheses through Self-Exploration", IEEE-RAS International Conference on Humanoid Robots (HUMANOIDS), 2014.
[50] Hinton, G.E., Salakhutdinov, R.R., "Reducing the dimensionality of data with neural networks", Science, 313(5786), 504-507, 2006.

reward function is also parameterized by the position of an obstacle in the camera frame, a policy will be computed to guide the arm passed the obstacle. Experiments will be conducted on a humanoid robot with targets detected using the system mentioned under Task 1.

3.1.3 Task 3: Grasp search and on-line stability assessment (month 48)

Finally, we will design a system that facilitates object grasping by detecting suitable grasp configurations for objects found using the system in Task 1. A search will be executed using a three-stage approach that first detects objects, then contact points on these objects, similarly to the work of Lenz et al.[18], and finally detects suitable grasp configurations for the highest ranked contact points, configurations expressed in terms of the joint angles of the arm and gripper. Each stage will be based on a separate deep network, but the structure of these networks will differ, with larger receptive fields for earlier stages.

For the last stage we envisage a deep network that allows inputs from vision, tactile as well as proprioceptive sensors, with the output being a predicted probability of grasp success. These modalities that might or might not be available at any point in time, depending on whether the gripper is in contact with the object or not. This is similar to an earlier system developed at CAS that was based on belief networks[31], but that system relied on a human operator to describe the shape of objects, instead of learning features relevant to the task automatically. With the ability to exploit modalities if and when they become available, grasp stability can be continuously assessed during grasping, so that failures can be predicted at an early stage and grasps be re-planned when needed.

For practical and safety reasons we intend to speed up the process of data collection by manually guiding the gripper towards possible grasp positions, even if this is a departure from our ambition to make the robot self-learn through exploration alone.

3.2 Work Package 2: Neuromorphic Robotics Sensory and Control System

In this work package we will develop a custom hardware solution for deep networks adapted for sensory processing and control with online learning. Input will be provided from WP1 as specifications on functional requirements, test cases for early simulation and dimensioning, and later for verification. Figure 2 shows a concept diagram of the custom Neuromorphic Robotics Sensory and Control System to be developed. The system has three components: a system controller, an external non-volatile memory to save the state of the system and a Dynamically Reconfigurable Neuromorphic Fabric (DRNF). The main research focus in this project will be the DRNF and we next present its salient features.

DRNF will be composed of Neuromorphic Cells (N-Cells) that each have a computational unit, a register File, a sequencer and interconnect elements necessary to build the fabric. The computational unit will have arithmetic to support the typical operations used in the targeted deep networks. The register file will serve as scratchpad for computation and have streaming capability. The sequencer will be used to program the streams from the register file and the memory banks, put the computational units in the right mode, program the interconnect to stream data from/to the right source/destination. The N-Cells will be interconnected by a circuit switched interconnect fabric. Besides the interconnect to glue the N-Cells into a fabric, another distributed interconnect scheme connecting the DRNF computational fabric to the 3D memory fabric will be designed to transfer data between register files and 3D memory fabric.

With technology scaling, the need for more memory capacity and bandwidth has become a fundamental architectural bottleneck, called memory wall, in achieving higher performance and computational efficiency[51]. Stacking DRAM in 3D above the computational die is the most direct way of addressing the memory capacity and memory bandwidth bottleneck[52]. For this reason, we propose using 3D stacking of DRAM in this project. The DRAM macros or D-

[51] McKee, S.A., "Reflections on the memory wall", In Proc. Conf. on Computing Frontiers, 2004.
[52] Loi, I. and Benini, L., "An efficient distributed memory interface for Many-Core Platform with 3D stacked DRAM", In Proc. Conf. on Design, Automation and Test in Europe, March 2010.

Tiles with streaming capability will be distributed on each die and will be interconnected by a 3D Network On Chip (NOC) with the DRNF computational. We intend to use circuit switch network, with its low overhead, because the traffic pattern remains static in terms of source and destination during processing of each deep network layer. To further reduce the memory overheads and the enhance the data transfer bandwidth, we will explore various compression mechanisms. The compression is also likely to reduce the energy consumption since the cost of storage and data transfer exceeds that of computation in modern chips. Prof. Hemani, along with his colleagues, pioneered the concept of NOCs in 2000[53] and the Electronic Systems group at KTH has considerable expertise in designing and dimensioning NOCs.

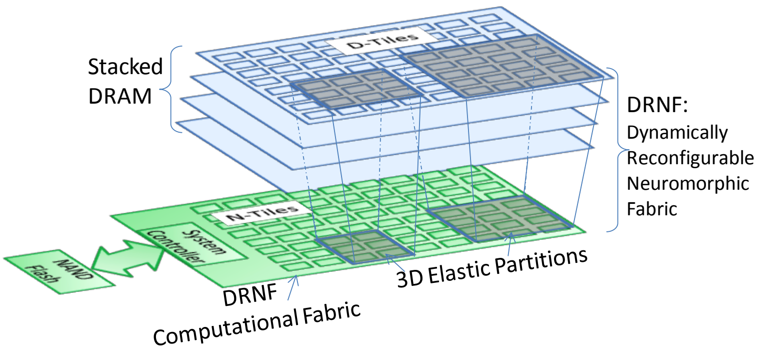

Figure 2 The Dynamically Reconfigurable Neuromorphic Fabric (DRNF)

The DRNF will have the ability to create elastic partitions, shown in Figure 2. A partition is a rectangular cluster of N-Cells and D-Tiles created by programming the interconnects. D-Tiles and register files would be programmed to stream data to the computational elements that are put in the right mode to perform a sequence of vector operations on multiple SIMD structures. Deploying such clusters of distributed computation and storage resources is key to achieve high computational efficiency. Elasticity and agility to dynamically create partitions is necessary for dealing with the varying computational requirements of different layers in the targeted deep networks from WP1. The creation of these partitions would be a distributed parallelized operation carried out by local sequencers in the N-Cells to ensure agility.

A compiler has been developed in the group of Prof. Hemani to target the coarse grain reconfigurable fabric DRRA. The compiler has adopted a pragma[54] based approach to identify the SIMDs and building a library of commonly used domain specific functions, with system level functionality expressed in terms of these pre-compiled library functions. We will adopt the same approach for DRNF and adapt the existing compiler framework for the proposed DRNF in this project.

3.2.1 Milestones for development of the neuromorphic hardware

- M1 (month 12): Technology to be used and architecture to be implemented defined.
- M2 (month 24): First hardware implementation, with DRRA compiler adapted for DRNF.
- M3 (month 36): Hardware synthesized down to physical level in 28nm technology node and prototyped in FPGAs. Functional verification of the hardware done. Transaction level model back-annotated with sign-off quality design data to be used to report computational efficiency. Results compared to the GPU and FPGA implementation.
- M4 (month 48): Final version of the algorithm and architecture implemented and verified. Detailed results in terms of performance and power metrics analysed. Roadmap for how this technology will evolve over coming years drawn and published.

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[53] Hemani, A., Jantsch, A., Kumar, S., Postula, A., Öberg, J., Millberg, M. and Lindqvist, M., "Network on a Chip: An architecture for billion transistor era", in Proc. Norchip Conference, 2000.

[54] Malik, O. and Hemani, A., "A Pragma Based Approach for mapping MATLAB Applications on a Coarse Grain Reconfigurable Architecture", in Proc. Symposium on Integrated Circuits and Systems Design, 2012

4 Personal Resources and International Collaboration

The proposed project will be led by Dr. Mårten Björkman in close collaboration with Prof. Ahmed Hemani. One doctoral student and one postdoctoral fellow will be deployed to carry out the project objectives. While both will collaborate on both work packages, the doctoral student will focus on WP1 and the postdoc on WP2. Funding from VR is only requested for the doctoral student, while the postdoc already has funding from KTH. Candidates for the project should have training in the areas of robotics, control theory, machine learning, computer vision and VLSI design. Prof. Danica Kragic will assist in co-supervision on robotic manipulation, together with Dr. Atsuto Maki on machine learning and Dr. Yasemin Bekiroglu on grasping. In terms of robotic platforms available for experimentation in the project, CAS has four robotic head-arm setups, including a PR2 humanoid robot with two arms and a robotic head, as well as five NAO humanoid robots.

CAS maintains a number of collaborations with international academic institutions in robotics and vision. Of interest for the project are on-going collaborations with UKE in Germany and UZH in Switzerland on computational sensorimotor modelling, Max Planck Institute in Germany on intelligent systems and SDU in Denmark on early visual models. The Electronic Systems group has extensive collaboration with Universities in India (IIT Delhi and IISc Bangalore) on massively parallel architectures and design methods. The group also collaborates with IMEC in Belgium on advanced memory management architectures and methods, with NTUA in Greece on distributed power management, with CEA-LETI in France on 3D integration and also in USA with UC Irvine and Penn State University.

5 Relevance, Significance & Impact

Representing and learning of sensorimotor relations on complex robotic systems with sensory and action spaces of high dimensionality is far from trivial. It has long been recognized, in computational biology, that neural networks can represent and learn such relations, but since the primary interest has been biological plausibility in modelling, not systems design, these models have been small in relation to those needed for robotics. Sensorimotor relations have been used for robotics by applying machine learning methods, but these have rarely been based on biologically sound models. It is widely believed that for robotic system to one day reach human levels of cognition many different research communities need to converge. The benefits of such collaborations can be fruitful indeed, which has recently been exemplified in large-scale object recognition tasks using deep neural networks. In NEUROACT we intend to explore the same benefits, but do so for robot control using sensorimotor relations and solve self-learning tasks, such as object reaching and grasping. For this to be possible we need computers targeted for the combined requirements of high performance, large memories and low power consumption.

The custom design, a configurable architecture for sensory processing and robot control with online learning, proposed in NEUROACT is the first such design as far as we know. Other proposed designs rely on offline learning or have a form factor and power consumption that is unsuitable for deployment on robots. Our design will enable deployment of brain-like computing for autonomous robots, and other embedded systems in industry and society. Though manufacturing costs of such designs tend to be high, by keeping them programmable, allowing high flexibility in functionality, large enough volume of end users can be generated and the manufacturing cost be amortized. History is full of engineering solutions, like mobile phones, that in the initial phase of their introduction have been expensive, but where high volumes have allowed prices to drop. We believe a similar phenomenon will accompany the solution proposed in this project. Swedish industry is a systems industry in all its sectors - defence, automotive, telecommunication, process control, robotics and manufacturing. All these industries are in need of machines with human like abilities and having this research done in Sweden will provide the Swedish Industry will a strategic advantage.

Interdisciplinarity

My application is interdisciplinary

☐

An interdisciplinary research project is defined in this call for proposals as a project that can not be completed without knowledge, methods, terminology, data and researchers from more than one of the Swedish Research Councils subject areas; Medicine and health, Natural and engineering sciences, Humanities and social sciences and Educational sciences. If your research project is interdisciplinary according to this definition, you indicate and explain this here.

Click here for more information

Scientific report

Scientific report/Account for scientific activities of previous project

Budget and research resources

Project staff

Describe the staff that will be working in the project and the salary that is applied for in the project budget. Enter the full amount, not in thousands SEK.

Participating researchers that accept an invitation to participate in the application will be displayed automatically under Dedicated time for this project. Note that it will take a few minutes before the information is updated, and that it might be necessary for the project leader to close and reopen the form.

Dedicated time for this project

	Role in the project	Name	Percent of full time
1	Applicant	Mårten Björkman	20
2	Participating researcher	Ahmed Hemani	15
3	Other personnel with doctoral degree	Asad Jafri	100

Salaries including social fees

	Role in the project	Name	Percent of salary	2016	2017	2018	2019	Total
1	Participating researcher	Mårten Björkman	20	164,000	168,000	172,000	177,000	681,000
2	Participating researcher	Ahmed Hemani	15	212,000	217,000	223,000	228,000	880,000
3	Other personnel without doctoral degree	Ny doktorand	80	427,000	470,000	517,000	568,000	1,982,000
	Total			803,000	855,000	912,000	973,000	3,543,000

Other costs

Describe the other project costs for which you apply from the Swedish Research Council. Enter the full amount, not in thousands SEK.

Premises

	Type of premises	2016	2017	2018	2019	Total
1	Offices	97,000	103,000	110,000	117,000	427,000
	Total	97,000	103,000	110,000	117,000	427,000

Running Costs

	Running Cost	Description	2016	2017	2018	2019	Total
1	Travel	Conferences	40,000	40,000	40,000	40,000	160,000
2	Computers and consumables	Hardware required for research	20,000	20,000	20,000	20,000	80,000
3	Publication fees		5,000	5,000	5,000	5,000	20,000
	Total		65,000	65,000	65,000	65,000	260,000

Depreciation costs

Depreciation cost	Description	2016	2017	2018	2019

Total project cost

Below you can see a summary of the costs in your budget, which are the costs that you apply for from the Swedish Research Council. Indirect costs are entered separately into the table.

Under Other costs you can enter which costs, aside from the ones you apply for from the Swedish Research Council, that the project includes. Add the full amounts, not in thousands of SEK.

The subtotal plus indirect costs are the total per year that you apply for.

Total budget

Specified costs	2016	2017	2018	2019	Total, applied	Other costs	Total cost
Salaries including social fees	803,000	855,000	912,000	973,000	3,543,000		3,543,000
Running costs	65,000	65,000	65,000	65,000	260,000		260,000
Depreciation costs					0		0
Premises	97,000	103,000	110,000	117,000	427,000		427,000
Subtotal	965,000	1,023,000	1,087,000	1,155,000	4,230,000	0	4,230,000
Indirect costs	417,000	444,000	474,000	505,000	1,840,000		1,840,000
Total project cost	1,382,000	1,467,000	1,561,000	1,660,000	6,070,000	0	6,070,000

Explanation of the proposed budget

Briefly justify each proposed cost in the stated budget.

Explanation of the proposed budget*

One doctoral student is planned to be employed with funding requested from VR. This student will work jointly with an postdoctoral fellow (Asad Jafri), who is financed through faculty funding from KTH, including overhead costs in terms of locales and indirect costs. These two will be supervised by faculty members, as stated in the proposal.

Salaries include "lönekostadspålägg" (53.20%), with an assumed annual increase in salaries by 10% for the doctoral student and 2.5% for faculty members. The total amount of overhead is 64.00%, which includes 12.07% for locales and 51.93% for indirect costs.

Other costs include those for publication of scientific reports, as well as for travelling to conferences and potential collaborators. Consumables include costs for program licenses and hardware that will become necessary for execution of the project.

Other funding

Describe your other project funding for the project period (applied for or granted) aside from that which you apply for from the Swedish Research Council. Write the whole sum, not thousands of SEK.

Other funding for this project

	Funder	Applicant/project leader	Type of grant	Reg no or equiv.	2016	2017	2018	2019	Total
1	KTH	Ahmed Hemani	Fakultetsmedel		1,082,000	1,109,000	1,137,000	1,164,000	4,492,00
	Total				1,082,000	1,109,000	1,137,000	1,164,000	4,492,00

CV

Curriculum Vitae

Name: Mårten Johan Björkman

Date of Birth: March 29, 1970

1 Higher education qualification

MSc Computer Science & Engineering (Civilingenjör Datateknik) LTH, SWEDEN 1994
Supervisor: Fredrik Dahlgren
Thesis: "Using Hints to Reduce the Read Miss Penalty for Flat COMA Protocols"

2 Degree of Doctor

PhD Computer Science (Teknologie Doktor Datalogi) KTH, SWEDEN 2002
Supervisor: Jan-Olof Eklundh
Thesis: "Real Time Motion and Stereo Cues for Active Visual Observers"

3 Post-doctoral positions

Czech Technical University, Czech Republic Center of Machine Perception (CMP) 2004

4 Qualification required for appointment as a docent

Docent in Computer Science KTH, SWEDEN 2013

5 Present Employment

Associate Professor ROYAL INSTITUTE OF TECHNOLOGY (KTH) since October 2011
School of Computer Science and Communications (CSC)
Research 45%, teaching 25%, administration 30%
Director of undergraduate studies in computer science

6 Previous Employment

Previous employment in academia:

Researcher KTH, SWEDEN May 2010–September 2011
Centre of Autonomous Systems (CAS), part time 40%
Researcher KTH, SWEDEN May 2007–April 2010
EC-IST project Paco-Plus, part-time 20%
Researcher KTH, SWEDEN May 2005–April 2007
EC-IST project MobVis, part-time 20%
Researcher KTH, SWEDEN January–April 2005
Department of Numerical Analysis and Computer Science (NADA)
Postdoctoral researcher KTH, SWEDEN July 2002–June 2004
EC-IST project CogVis
Doctoral student KTH, SWEDEN August 1997–June 2002
Department of Numerical Analysis and Computer Science (NADA)

Previous employment in industry:

Head of research OCULUSAI TECHNOLOGIES AB, SWEDEN — Febuary 2010–September 2011
part time 60-80%

Product manager INTELLIGENT MOBILE DOCUMENTATION AB, SWEDEN — April 2005–January 2010
Co-founder, part-time 80%, sold to Unwire Group 2013

Application engineer MENTOR GRAPHICS AB, SWEDEN — September 1994–July 1997
Digital signal processing, low power IC design

7 Interruption in research

Paternity leave 80% — March 2012-September 2012

Oculus Technologies AB 60% — Febuary 2010–September 2011

Intelligent Mobile Documentation AB 80% — April 2005–January 2010

Intelligent Mobile Documentation AB 100% — July 2004–September 2004

8 Supervision

Ali Gadhirzadeh PhD student, main supervisor — since 2013

Rasmus Göransson PhD student, co-supervisor — since 2013

Javier Gratal PhD student, co-supervisor — since 2013

Virgile Högman PhD student, co-supervisor — since 2012

Niklas Bergström PhD (graduated), co-supervisor — 2008–2012

Babak Rasolzadeh PhD (graduated), co-supervisor — 2005–2011

9 Awards

Best Cognitive Robotics paper Finalist IROS 2013
"Enhancing visual perception of shape through tactile glances"

Best Cognitive Robotics paper Winner IROS 2011
"Generating object hypotheses in natural scenes through human-robot interaction"

CV of Ahmed Hemani (610308-2290)
Bilaga B

1. Högskoleexamen

1982, Electrical and Electrical Engineering. University of Indore, India.

2. Doktorsexamen

1993, Applied Electronics, KTH, Stockholm, Sweden. Title: "High-Level Synthesis of Synchronous Digital Systems using Self-Organization based Scheduling and Binding. Supervisors: Dr. Adam Postula.

3. Post Doc: None

4. Docentkompetens

Associate Professor in September 1994 and Docent in the year 1998, both at KTH.

5. Nuvarande anställning

Professor since August 2005 at Department of Electronic Systems, School of Information and Communications Technology, KTH, Kista, Sweden. 85% Research and 15% Education.

Lead a group 8 active PhD students working on high performance, massively parallel architectures and design methods for wireless signal processing applications. A related work on Globally Ratiochronous and Locally Synchronous clocking and distributed power management for massively parallel architectures. Another related project is on massively parallel custom architectures for bioinformatics applications.

6. Tidigare anställningar och förordnandetider

Sept 1994 - June 2000.

Associate Professor, KTH, Kista, Sweden. (Part Time)

Responsible for a) graduate students, b) undergraduate and graduate education in the area of Electronic System Design. Formulation, c) fund raising and management of research projects in the area of Design Methods and Tools for VLSI systems and d) Research ASIC projects in collaboration with Industry like Ericsson and Bofors

July 1997 - October 2000.

Consultant ASICs Designer. Ericsson Radio Systems. (Part Time).

Contributed to design and verification of ASICs/SOCs for GSM basestations.

May 1993 - Sep. 1994.

Senior Scientist. KTH, Kista, Sweden.

Contributed to undergraduate education and research in the area of Electronics Systems Design.

Dec 1986 - Jan 1993.

Swedish Institute of Micro-electronics/Synthesia. (Part Time)

Research in Electronics Systems Design. Especially Logic and High-Level Synthesis.

Jan 1988 - Apr. 1993.

KTH, Kista, Sweden. (Part Time)

The applicant was a member of Technical Staff at Swedish Institute of Micro-electronics, Kista, Sweden and since Jan. 1988 a PhD student at KTH. He did research in the area of Logic Synthesis and his PhD research was about High-Level Synthesis. This resulted in a system called SYNT that was commercialized by Synthesia which was acquired by CADENCE.

Apr. 1984 - Dec. 1986.

ABB, Västerås, Sweden.

Member of Technical Staff. Contributed to Design of ASEA Process Control Systems and Man Machine Communication Systems. Porposed and prototyped Transputer/Occam based Process control Systems

Aug. 1982 - Mar. 1984.

Digital Innovations Ltd, Vadodara, India.

Member of Technical Staff. Contributed to development of cross-development environment for Nationals NS32000 CISC processors, specifically responsible for Symbolic Debugger. Responsible for quality assurance test of this development suite at National's Sunnyvale site.

7. Uppehåll i forskningen (1997-2005). (For the period Jul 1997-Oct 2000 see above.)

September 2004-October 2005.

System Architect at Philips Semiconductors, Eindhoven, The Netherlands. Principle architect for Philips' flagship Multimedia Wireless Processor in 65 nm technology. Represented Philips in the SPIRIT consortium - an industrial consortium to standardize exchange and reuse of IPs in an XML based format (now known as IP-XACT).

August 2003 - July 2004.

Consultant Senior ASIC Designer at NewLogic Technologies, Sophia Antipolis, France.

Contributed to design and implementation of NewLogic's WLAN family of IPs, RF front end (digital part) and Modem for the 802.11a/g standards.

October 2000 - July 2003.

ASIC Design Manager, Spirea AB, Kista, Sweden

Responsible for the digital design of Bluetooth Physical Layer, Baseband and System Level Modelling of WLAN. Co-author of a patent for Linearization of Power Amplifier.

8. Personer som avlagt doktorsexamen

So far supervised eight PhDs and two Licentiates. Five more PhDs and one Licentiate are due to finish during next two years.

9. Research Career Summary

VLSI Design Methods and Tools:

1. Logic Synthesis,
2. High-Level Synthesis. *Doctoral Thesis on High-Level Synthesis was commercialized by CADENCE as Visual Architect*.
3. Hardware Software Co-design, System Level Synthesis from SDL, Matlab, Simulink
4. Grammar Based Design Methods, and Meta Models for analyzing VLSI concepts.
5. System Level Synthesis for massively parallel coarse grain reconfigurable fabrics.

VLSI Architectures:

1. Globally Asynchronous Locally Synchronous Architectures. *This work has been done in collaboration with Ericsson and has been adopted by TI and Ericsson*.
2. Networks On Chip: *Pioneered this concept and wrote the first paper to use the term Networks-on-Chip.*
3. Massively Parallel Coarse Grain Reconfigurable Architecture for Wireless and Bioinformatics applications

Radio Systems Design. Robust Bluetooth Physical Layer, Linearization of Power Amplifier. RF/Analog impairment and channel modeling and testbed for realtime emulation.

Funding: Between 1988-2012 principal applicant for 40 MSEK research funding.

Publications:

1. 175 peer reviewed conference and journal publications, invited Chapters in Books.
2. 3 Patents
3. H-Index: 17. i10 Index: 26. Citation Count: 2626. (Google Scholar)

10. Postdoctoral researchers/Visiting Professors/Collaborators

The applicant has had active collaboration with Prof. Alberto Sangionvanni Vincentelli, UC Berkeley; arranged an exchange visit of a PhD student to Prof. Vincentelli's lab at UCB. Prof. Rolf Ernst, Univ. of Braunshweig, Germany. Prof. Francky Cathoor, IMEC, Belgium. Prof. Dimitrios Dsoudris, NTUA, Greece. Prof. Anshul Kumar, IIT Delhi, Prof. Adam Postula, Univ. of Queensland, Australia. Dr. Kolin Paul, IIT Delhi. Prof. S K Nandy, Indian Institute of Science, Bangalore, India.

11. Conference Program Committees, Review

The applicant has been part of the Program Committees for VLSI Design, DATE, DAC, DSD, Euromicro and BEC.

The applicant has reviewed many IEEE VLSI Transaction Journal Papers, especially on High-Level Synthesis and Low Power Design. Co-organized Multi Core Conference, Kista in 2012 and Multi-core Embedded Systems Workshop, co-located with ISCAS 2013.

12. Invited Presentations

The applicant has given invited presentations on Trends in SOC Design, Coarse Grain Reconfigurable Architectures and Massively Parallel Machines, Globally Asycnhronous Locally Synchronous Design and Distributed Power Management at Beijing Union Universtiy, IIT Delhi, RAMSIS Summer School, Visby, Gotland (SSF funded project).

Publication list

Publications - Mårten Björkman

Publication from the last 8 years, including the 5 most cited papers. The number of citations below are the Google Scholar counts. Scientific impact: *h-index 13, Citation count: 641*.

1 Most cited papers

[1] P. Jensfelt, D. Kragic, J. Folkesson and M. Björkman, "A Framework for Vision Based Bearing Only 3D SLAM", in Proc. IEEE International Conference on Robotics and Automation (ICRA), Orlando, USA, pp. 1944-1950, May 2006. **Number of citations: 103**

[2] D. Kragic, M. Björkman, H.I. Christensen and J-O. Eklundh, "Vision for Robotic Object Manipulation in Domestic Settings", *Robotics and Autonomous Systems, 52(1), pp. 85-100, July 2005.* **Number of citations: 86**

[3] B. Rasolzadeh, M. Björkman, K. Huebner and D. Kragic, "An active vision system for detecting, fixating and manipulating objects in real world", *International Journal of Robotics Research, 29(2-3), 2010.* **Number of citations: 72**

[4] M. Björkman and D. Kragic, "Active 3D Scene Segmentation and Detection of Unknown Objects", in Proc. International Conference on Robotics and Automation (ICRA), May 2010. **Number of citations: 57**

[5] M. Björkman and D. Kragic, "Combination of Foveal and Peripheral Vision for Object Recognition and Pose Estimation", in Proc. International Conference on Robotics and Automation (ICRA), Apr 2004. **Number of citations: 42**

2 Internationally Peer Reviewed Journal Articles

[1] M. Björkman, N Bergström, D Kragic "Detecting, segmenting and tracking unknown objects using multi-label MRF inference", *Computer Vision and Image Understanding*, 118, pp. 111-127, 2014. **Number of citations: 2**

[2] * B. Rasolzadeh, M. Björkman, K. Huebner and D. Kragic, "An active vision system for detecting, fixating and manipulating objects in real world", *International Journal of Robotics Research, 29(2-3), 2010.* **Number of citations: 72**

3 Internationally peer reviewed conference publications

[3] * M. Björkman, Y. Bekiroglu and D Kragic, "Learning to Disambiguate Object Hypotheses through Self-Exploration", in IEEE-RAS International Conference on Humanoid Robots (HUMANOIDS), Madrid Sprain, Nov 2014.

[4] I. Lundberg, P. Ögren and M. Björkman, "Intrinsic Camera and Hand-Eye Calibration for a Robot Vision System using a Point Marker", in IEEE-RAS International Conference on Humanoid Robots (HUMANOIDS), Madrid Sprain, Nov 2014.

[5] * A. Ghadirzadeh, G. Kootstra, A. Maki and M. Björkman, "Learning visual forward models to compensate for self-induced image motion" in Proc. IEEE International Symposium on Robot and Human Interactive Communication (RO-MAN), Edinburgh, UK, Aug 2014.

[6] F. Pokorny, Y. Bekiroglu, J. Exner, M. Björkman and D. Kragic, "Grasp Moduli Spaces, Gaussian Processes, and Multimodal Sensor Data", in Proc. Workshop on Information-based Grasp and Manipulation Planning, Robotics: Science and Systems, Berkeley, USA, Jul 2014.

[7] * M. Björkman, Y. Bekiroglu, V. Högman and D. Kragic, "Enhancing visual perception of shape through tactile glances", in Proc. IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), Tokyo, Japan, Sep 2013. **Number of citations: 4**

[8] * V. Högman, M. Björkman and D. Kragic, "Interactive object classification using sensorimotor contingencies", in Proc. IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), Tokyo Japan, Sep 2013. **Number of citations: 3**

[9] X. Gratal, C. Smith, M. Björkman and D. Kragic, "Integrating 3D Features and Virtual Visual Servoing for Hand-Eye and Humanoid Robot Pose Estimation", in Proc. IEEE-RAS International Conference on Humanoid Robots (HUMANOIDS), Atlanta, USA, Sep 2013.

[10] L. Nalpantidis, M. Björkman and D. Kragic, "YES-YEt Another Object Segmentation: Exploiting Camera Movement", in Proc. IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), Algarve, Portugal, Oct 2012. **Number of citations: 1**

[11] N. Bergström, M. Björkman and D. Kragic, "Generating object hypotheses in natural scenes through human-robot interaction", in Proc. IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), San Fransisco, USA, Sep 2011. **Number of citations: 24**

[12] N. Bergström, C. Ek, M. Björkman and D. Kragic, "Scene understanding through autonomous interactive perception", in Proc. International Conference on Computer Vision Systems (ICVS), Sophia Antipolis, France, Sep 2011. **Number of citations: 10**

[13] J. Bohg, M. Johnson-Roberson, M. Björkman and D. Kragic, "Strategies for Multi-Modal Scene Exploration", in Proc. IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), Taipei, Taiwan, Oct 2010. **Number of citations: 8**

[14] M. Johnson-Roberson, J. Bohg, M. Björkman and D. Kragic, "Attention based Active 3D Point Cloud Segmentation", in Proc. IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS), Taipei, Taiwan, Oct 2010. **Number of citations: 23**

[15] X. Gratal, J. Bohg, M. Björkman and D. Kragic, "Scene Representation and Object Grasping Using Active Vision" in Proc. Workshop on Defining and Solving Realistic Perception Problems in Personal Robotics, Taipei, Taiwan, 2010. **Number of citations: 7**

[16] M. Björkman and D. Kragic, "Active 3D Scene Segmentation and Detection of Unknown Objects", in Proc. International Conference on Robotics and Automation (ICRA), May 2010. **Number of citations: 57**

[17] M. Björkman and D. Kragic, "Active 3D Segmentation through Fixation of Previously Unseen Objects", in Proc. British Machine Vision Conference (BMVC), Aberystwyth, UK, Sep 2010. **Number of citations: 17**

[18] K. Huebner, M. Björkman, B. Rasolzadeh, M. Schmidt and D. Kragic, "Integration of Visual and Shape Attributes for Object Action Complexes", in Proc. International Conference on Computer Vision Systems (ICVS), pp. 13-22, Santorini, Greece, May 2008. **Number of citations: 10**

Ahmed Hemani. (610308-2290)
Neuromorphic architectures for sensorimotor couplings on robots
Bilaga C - Publications List for last 8 years

H-Index: 17. i10 Index: 26. Citation Count: 2626. (Google Scholar was used for citation count)

1. Five most cited publications

1. S Kumar, A Jantsch, JP Soininen, M Forsell, M Millberg, J Oberg. "A network on chip architecture and design methodology" Proceedings. IEEE Computer Society Annual Symposium on VLSI, 2002. 105-112. Number of Citations: 1093
2. A Hemani, A Jantsch, S Kumar, A Postula, J Oberg, M Millberg. "NETWORK on chip: An architecture for billion transistor era". Proceeding of the IEEE NorChip Conference, 2000. Number of Citations: 387
3. A Hemani, T Meincke, S Kumar, A Postula, T Olsson, P Nilsson, J Oberg. "Lowering power consumption in clock by using globally asynchronous locally synchronous design style". Design Automation Conference, 1999. Proceedings. 36th, 873-878, 1999. Number of Citations: 168
4. A Jantsch, P Ellervee, A Hemani, J Öberg, H Tenhunen. "Hardware/software partitioning and minimizing memory interface traffic". Proceedings of the conference on European design automation, 226-231,1994. Number of Citations: 116
5. A Jantsch, P Ellervee, Johnny Oberg, A Hemani. "A case study on hardware/software partitioning". Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, 1994. Number of Citations: 75

2. Peer-reviewed Articles (Journal publications.)

1. S. Penolazzi, A. Hemani and L. Bolognino, "A General Approach to High-Level Energy and Performance Estimation in SoCs", in Journal of Low Power Electronics (JOLPE), Volume 5, Number 3, December 2009, Number of Citations: 5
2. Haider Abbas, Christer Magnusson, Louise Yngström and Ahmed Hemani. Addressing dynamic issues in information security management. Informantion Managment and Computer Security. ISSN 0968-5227. Volume 19, Number 1 2011, Number of Citations: 4
3. (*)Chabloz, J.-M.; Hemani, A., "Low-Latency Maximal-Throughput Communication Interfaces for Rationally Related Clock Domains," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.22, no.3, pp.641,654, March 2014, Number of Citations: 1
4. *Jafri Syed Mohammad Asad Hassan, Hemani Ahmed*. Energy-aware Fault-tolerant Network-on-chips for Addressing Multiple Traffic Classes. Microprocessors and Microsystems, Elsevier, 2013.
5. Nasim Farahini, Ahmed Hemani, Hassan Sohofi, Seyed M. A. H. Jafri, Muhamamd Adeel Tajammul, Kolin Paul, "Parallel Distributed Scalable Address Generation Scheme for a Coarse Grain Reconfigurable Computation and Storage Fabric," Journal of Microprocessors and Microsystems, 2014.
6. (*)Syed M. A. H. Jafri, Muhammad Adeel Tajammul, Ahmed Hemani, Juha Plosila, Hannu Tenhunen: Morphable configuration architecture to address multiple reconfiguration needs. IEEE Transaction on VLSI (accepted)
7. (*)Syed M. A. H. Jafri, Ozan Ozbak, Ahmed Hemani, Nasim Farahini, Kolin Paul, Juha Plosila, Hannu Tenhunen: Architecture and Implementation of Dynamic Parallelism, Voltage, and Frequency Scaling on CGRAs, ACM JETC (accepted)
8. Syed M. A. H. Jafri, Stanislaw Piestrak, Kolin Paul, Ahmed Hemani, Juha Plosila, Hannu Tenhunen: Private reliability environments for efficient fault-tolerance in CGRAs, Springer Design Automation for Embedded Systems. 2013

2. **Peer-reviewed Conference publications.**

9. *Penolazzi, Sandro; Hemani, Ahmed;* A Layered Approach to Estimating Power Consumption. In the Proceedings of the NORCHIP Conference, November 2006, Linkköping, Number of Citations: 3
10. *Penolazzi Sandro, Badawi Mohammed, Hemani Ahmed*; Modelling Embedded Systems at Functional Untimed Application Level. IP-SOC 2007, November 2007, Grenoble France.
11. *S. Penolazzi, M. Badawi, and A. Hemani,* "A Step Beyond TLM Inferring Architectural Transactions at Functional Untimed Level", in VLSI-SoC, Rhodes, Greece, 2008, Number of Citations: 4
12. *Asad Raza, Abbas Haider, Louise Yngstrom, Ahmed Hemani,* Security evaluation of esam architecture using atam, IPID 2008, FINLAND
13. *S. Penolazzi, A. Hemani and L. Bolognino,* "A General Approach to High-Level Energy and Performance Estimation in SoCs", in VLSI, New Delhi, India, 2009, Number of Citations: 5
14. *S. Penolazzi, L. Bolognino and A. Hemani,* "Energy and Performance Model of a SPARC Leon3 Processor", in Euromicro DSD, Patras, Greece, 2009, Number of Citations: 6
15. *Jean-Michel Chabloz, Ahmed Hemani,* "A Flexible Communication Scheme for Rationally-Related Clock Frequencies," in Proceedings of the 27th International Conference of Computer Design, 2009, Number of Citations: 20
16. *Abbas, Haider, Louise Yngstrom, Ahmed Hemani,* Security evaluation of Products: Bridging The Gap Between Common Criteria (Cc) And Real Option Thinking, Wcecs 2008, San Francisco USA, Number of Citations: 3
17. Abbas Haider, Louise Yngstrom, Ahmed Hemani, Option Based Evaluation: Security Evaluation Based On Options Theory, IEEE ECBS-EERC 2009, NOVI SAD, SERBIA, Number of Citations: 3
18. Abbas Haider, Louise Yngstrom, Ahmed Hemani, Poster: empowering security evaluation of it products by real options theory, IEEE Security And Privacy 2009, CALIFORNIA, USA
19. Asad Raza, Abbas Haider, Louise Yngstrom, Ahmed Hemani, Security Characterization For Evaluation Of Software Architectures Using Atam, IEEE ICIT 2009, KARACHI, PAKISTAN, Number of Citations: 4
20. Abbas, Haider, Louise Yngstrom, Ahmed Hemani, Adaptability model Development for it security evaluation based on options theory, IEEE ACM SIN 2009, CYPRUS.
21. Shami, M.A.; Hemani, A., "Morphable DPU: Smart and efficient data path for signal processing applications," *Signal Processing Systems, 2009. SiPS 2009. IEEE Workshop on* , vol., no., pp.167,172, 7-9 Oct. 2009, Number of Citations: 17
22. *Muhammed Ali Shami, Ahmed Hemani.* Partially Reconfigurable Interconnection Network for Dynamically Reprogrammable Resource Array in IEEE 8th International Conference on ASIC, October 20-23, 2009, Number of Citations: 16
23. *Jamshaid Malik, Ahmed Hemani.* On the design of Doppler filters for next generation radio channel simulators.. 3rd International Conference on Signals, Circuits and Systems (SCS), 2009. Publication Year: 2009 , Page(s): 1 - 6, Number of Citations: 2
24. *S. Penolazzi, I. Sander and A. Hemani*, "Predicting Energy and Performance Overhead of Real-Time Operating Systems". In DATE10, Dresden, Germany, 2010, Number of Citations: 2
25. *Jean-Michel Chabloz, Ahmed Hemani,* "Distributed DVFS Using Rationally-Related Frequencies and Discrete Voltage Levels. ISLEPD, 18-10 August 2010, Austin USA, Number of Citations: 19
26. *Pei Liu and Ahmed Hemani,* "Coarse Grain Reconfigurable Architecture for Sequence Alignment

Problems in Bio-informatics", SASP June 13-14 2010, Anahein USA, Number of Citations: 3

27. *Jamshaid Malik, Ben Slimane, Ahmed Hemani, N D Gohar,* "Impact of Interpolation Techniques on Statistical Properties and Speed of Fading Channel Simulators, ICWMC-Sept 2010, Barcelona Span.

28. *Sandro Penolazzi, Ingo Sander, Ahmed Hemani,* "Inferring Energy and Performance Cost of RTOS in Priority-Driven Scheduling", SIES Sept 2010 Italy, Number of Citations: 1

29. *Jean-Michel Chabloz, Ahmed Hemani,.* Lowering the Latency of Interfaces for Rationally-Related Frequencies. ICCD October 2010, Number of Citations: 6

30. *Muhammed Ali Shami, Ahmed Hemani.* Control Scheme in a Coarse Grain Reconfigurable Architecture. 22nd Intl Symposium on Computer Architecture and High Performance Computing, Brasil Oct. 27-30 2010.

31. *Omer Malik, Ahmed Hemani.* A Library Development Framework for a Coarse Grain Reconfigurable Architecture. VLSI Design, Chennai. India. 2011, Number of Citations: 9

32. *Adeel Tajammul, Ahmed Hemani.* NoC Based Distributed Partitionable Memory System for a Coarse Grain Reconfigurable Architecture.VLSI Design, Chennai. India. 2011, Number of Citations: 4

33. *Abbas Haider, Christer Magnusson, Louise Yngström, Ahmed Hemani,* "Architectural Description of an Automated System for Uncertainty Issues Management in Information Security", International Journal of Computer Science and Information Security, USA, Vol. 8 No. 3, June 2010, pages 59-67

34. *Abbas Haider, Christer Magnusson, Louise Yngström, Ahmed Hemani,* "A Structured Approach for Internalizing Externalities Caused by IT Security Mechanisms", in Proceedings of IEEE International Workshop on Education Technology and Computer Science (ETCS 2010), March 6-7, 2010, Wuhan, China, pages 149-153, Number of Citations: 3

35. Pei Liu; Hemani, A.; Paul, K., "A Reconfigurable Processor for Phylogenetic Inference," *VLSI Design (VLSI Design), 2011 24th International Conference on* , vol., no., pp.226,231, 2-7 Jan. 2011, Number of Citations: 1

36. *Omer Malik, Ahmed Hemani*. High Level Synthesis Framework For a Coarse Grain Reconfigurable Architecture. NORCHIP Nov. 2010. Tampere Finland, Number of Citations: 4

37. *Li Shuo, Fahimeh Jafri, Shashi Kumar, Ahmed Hemani.* Layered Spiral Algorithm for Memory-Aware Mapping and Scheduling on Network-on-Chip. NORCHIP Nov. 2010. Tampere Finland, Number of Citations: 1

38. *Ali Shami, Ahmed Hemani.* Implementation Exploration for a Self Reconfigurable Interconnection Network in DRRA. NORCHIP Nov. 2010. Tampere Finland.

39. *Mohammed Adeel Tajammul, Sri Moorthi, Ahmed Hemani.* A NoC Based Distributed Memory Architecture with Programmable and Partitionable Capabilities. NORCHIP Nov. 2010. Tampere Finland, Number of Citations: 3

40. Candaele, B.; Aguirre, S.; Sarlotte, M.; Anagnostopoulos, I.; Xydis, S.; Bartzas, A.; Bekiaris, D.; Soudris, D.; Zhonghai Lu; Xiaowen Chen; Chabloz, J.; Hemani, A.; Jantsch, A.; Vanmeerbeeck, G.; Kreku, J.; Tiensyrja, K.; Ieromnimon, F.; Kritharidis, D.; Wiefrink, A.; Vanthournout, B.; Martin, P., "Mapping Optimisation for Scalable Multi-core ARchiTecture: The MOSART Approach," *VLSI (ISVLSI), 2010 IEEE Computer Society Annual Symposium on* , vol., no., pp.518,523, 5-7 July 2010, Number of Citations: 3

41. *Jamshaid Sarwar Malik, Ben Slimane, Ahmed Hemani, N D Gohar*. Improving Performance of Fading Channel Simulators by use of Uniformly Distributed Random Numbers. IEEE International Symposium on Signal Processing and Information Technology. December 15-18, 2010 - Luxor - Egypt.

42. *Jafri, S.M.A.H., Hemani, A.; Paul, K.; Plosila, J.; Tenhunen, H.*; , "Compression Based Efficient

and Agile Configuration Mechanism for Coarse Grained Reconfigurable Architectures," IEEE International Symposium on Parallel and Distributed Processing Workshops and Phd Forum (IPDPSW), 2011, vol., no., pp.290-293, 16-20 May 2011. Digital Id: 10.1109/IPDPS.2011.166, Number of Citations: 3

43. *Muhammad Ali Shami and Ahmed Hemani*. Address Generation Scheme for a Coarse Grain Reconfigurable Architecture. ASAP 2011 — 22nd IEEE International Conference on Application-specific Systems, Architectures and Processors. Santa Monica, California, USA, September 11-14, 2011, Number of Citations: 7
44. Jafri, S.M.A.H.; Hemani, A.; Paul, K.; Plosila, J.; Tenhunen, H., "Compact generic intermediate representation (CGIR) to enable late binding in coarse grained reconfigurable architectures," *Field-Programmable Technology (FPT), 2011 International Conference on* , vol., no., pp.1,6, 12-14 Dec. 2011, Number of Citations: 8
45. *Mohammad Badawi and Hemani Ahmed.* A Coarse-Grained Reconfigurable Protocol Processor. SOC 2011, Tampere, Finland. November 2011, Number of Citations: 1
46. Omer Malik and Ahmed Hemani. Synchronizing Distributed State Machines In A Coarse Grain Reconfigurable Architecture. SOC 2011, Tampere, Finland. November 2011, Number of Citations: 2
47. Pei Liu, Ahmed Hemani and Kolin Paul, “A Reconfigurable Processor for Phylogenetic Inference,” in 24th International Conference on VLSI Design (VLSI Design), 2011, Number of Citations: 1
48. Pei Liu; Ebrahim, F.O.; Hemani, A.; Paul, K.; , "A Coarse-Grained Reconfigurable Processor for Sequencing and Phylogenetic Algorithms in Bioinformatics," Reconfigurable Computing and FPGAs (ReConFig), 2011 125. International Conference on, pp.190-197, 2011, Number of Citations: 3
49. Penolazzi, S.; Sander, I.; Hemani, A.;. Predicting bus contention effects on energy and performance in multi-processor SoCs, Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011, Number 127. of Citations: 2
50. Fahimeh Jafari, Shuo Li, and Ahmed Hemani. Optimal Selection of Function Implementation in a Hierarchical Configware Synthesis Method for a Coarse Grain Reconfigurable Architecture. in DSD 2011: 14th 122. EUROMICRO CONFERENCE ON DIGITAL SYSTEM DESIGN. Aug 31-Sept 2 2011, Oulu, Finland, Number of Citations: 3
51. Jean-Michel Chabloz and Ahmed Hemani. A GALS Network-on-Chip based on Rationally-Related Frequencies. ICCD October 2011, Number of Citations: 1
52. Li Shuo, Guo Chen, Ahmed Hemani. A Code Reuse Method for Many-Core Coarse-Grained Reconfigurable Architecture Function Library Development, 2011 International Symposium on Integrated Circuits. Singapore, December 2011, Number of Citations: 2
53. Chabloz, Jean-Michel, Hemani, Ahmed. Low-Latency and Low-Overhead Mesochronous and Plesiochronous Synchronizers,” in DSD 2011: 14th EUROMICRO Conference on Digital System Design. Aug 31-Sept 2 2011, Oulu, Finland, Number of Citations: 2
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55. Jamshaid S. Malik, Jameel Malik, A Hemani, N.D Gohar, “An Efficient Hardware implementation of High Quality AWGN Generator Using Box-Muller Method”, IEEE ISCIT , Hangzhou, China, 2011, Number of Citations: 3
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57. Chabloz, J.-M.; Hemani, A., "Low-Latency No-Handshake GALS Interfaces for Fast-Receiver Links," VLSI Design (VLSID), 2012 25th International Conference on , vol., no., pp.191,196, 7-11 Jan. 2012
58. Jamshaid Sarwar Malik, Paolo Palazzari, and Ahmed Hemani. 2012. Effort, resources, and abstraction vs performance in high-level synthesis: finding new answers to an old question. SIGARCH Comput. Archit. News 40, 5 (March 2012), 64-69.
59. Shami, M.A.; Hemani, A., "Classification of Massively Parallel Computer Architectures," Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW), 2012 IEEE 26th International , vol., no., pp.344,351, 21-25 May 2012, Number of Citations: 4
60. Pei Liu; Hemani, A.; Paul, K., "Improved Bioinformatics Processing Unit for Multiple Applications," Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW), 2012 IEEE 26th International , vol., no., pp.390,396, 21-25 May 2012
61. Malik, O.; Hemani, A., "A pragma based approach for mapping MATLAB applications on a coarse grained reconfigurable architecture," Integrated Circuits and Systems Design (SBCCI), 2012 25th Symposium on , vol., no., pp.1,6, Aug. 30 2012-Sept. 2 2012, Number of Citations: 1
62. Jafri, S.M.A.H.; Liang Guang; Hemani, A.; Paul, K.; Plosila, J.; Tenhunen, H., "Energy-Aware Fault-Tolerant Network-on-Chips for Addressing Multiple Traffic Classes," Digital System Design (DSD), 2012 15th Euromicro Conference on , vol., no., pp.242,249, 5-8 Sept. 2012, Number of Citations: 3
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64. Jafri, S.M.A.H.; Bag, O.; Hemani, A.; Farahini, N.; Paul, K.; Plosila, J.; Tenhunen, H., "Energy-aware coarse-grained reconfigurable architectures using dynamically reconfigurable isolation cells," Quality Electronic Design (ISQED), 2013 14th International Symposium on , vol., no., pp.104,111, 4-6 March 2013
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66. Farahini, N.; Hemani, A., "A conceptual custom super-computer design for real-time simulation of human brain," Electrical Engineering (ICEE), 2013 21st Iranian Conference on , vol., no., pp.1,6, 14-16 May 2013
67. Farahini, N.; Shuo Li; Tajammul, M.A.; Shami, M.A.; Guo Chen; Hemani, A.; Wei Ye, "39.9 GOPs/watt multi-mode CGRA accelerator for a multi-standard basestation," Circuits and Systems (ISCAS), 2013 IEEE International Symposium on , vol., no., pp.1448,1451, 19-23 May 2013, Number of Citations: 2
68. Nidhi, U.; Paul, K.; Hemani, A.; Kumar, A., "High performance 3D-FFT implementation," Circuits and Systems (ISCAS), 2013 IEEE International Symposium on , vol., no., pp.2227,2230, 19-23 May 2013
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71. Shuo Li; Hemani, A., "Memory allocation and optimization in system-level architectural

synthesis," Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC), 2013 8th International Workshop on , vol., no., pp.1,7, 10-12 July 2013

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73. Jafri, S.M.A.H.; Piestrak, S.J.; Paul, K.; Hemani, A.; Plosila, J.; Tenhunen, H., "Energy-Aware Fault-Tolerant CGRAs Addressing Application with Different Reliability Needs," Digital System Design (DSD), 2013 Euromicro Conference on , vol., no., pp.525,534, 4-6 Sept. 2013, Number of Citations: 1
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76. (*)Shuo Li; Farahini, N.; Hemani, A.; Rosvall, K.; Sander, I., "System level synthesis of hardware for DSP applications using pre-characterized function implementations," Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2013 International Conference on , vol., no., pp.1,10, Sept. 29 2013-Oct. 4 2013
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80. (*)Tuan Nguyen, Syed M. A. H. Jafri, Sergei dyctrov, Masoud Daneshtalab, Ahmed Hemani, Juha Plosila, Hannu Tenhunen: FIST: A Framework to Interleave Spiking neural networks on CGRAs. International Conference on Parallel, Distributed and network based computing (PDP) February 2015, Turku, Finland.

3. Review Articles, book chapters, books

81. *Hemani, A, Klapproth, P*. Trends in SOC Architectures. Chapter in the book “Radio Design in Nanonmeter Technologies” Edited by Professor Mohammed Ismail and Delia Gonzales. Published by Springer Verlag in Summer 2006.
82. *Jean Michel Chabloz, Ahmed Hemani* Chapter 3: Power Management Architectures in McNOC. Chapter in the book “Scalable Multi-Core Architectures” Edited by Prof. Axel Jantsch and Prof. Dimitrios Soudris. Springer. ISBN 978-1-4419-6777-0. e-ISBN 978-1-4419-6778-7.

4. Patents

83. *Tommy Öberg, Ahmed Hemani, Daniel Björk.* Envelope Elimination and Restoration Device. US Patent Application Nr. 20050002469
84. A Programmable Controller, Axel Jantsch, Ahmed Hemani, Xiaowen Chen, Zhonghai Lu, International Patent Applications PCT/SE2009/050872, under submission.

85. Asynchronous Interface. Jean Michel Chabloz, Ahmed Hemani. Patent Application PCT/SE2010/051439

5. Software Programs and Hardware IPs

1. DRRA – Dynamically Reconfigurable Resource Array is a Coarse Grain Reconfigurable Fabric
2. DiMARCH – is a complementary partitionable distributed memory fabric that is complement to DRRA
3. VESYLA – is a High Level Synthesis tool for mapping C/Matlab functions to the DRRA and DiMARCH
4. SYLVA – is System Level Architectural Synthesis tool for mapping complete Modem and Codec sub-systems to the DRRA and DiMARCH fabrics, ASICs and FPGAs.
5. eBrain – a multi-chip custom supercomputer for real time simulation of an abstract model of a human scale cortex.

CV

Name: Mårten Björkman	**Doctorial degree:** 2002-06-14
Birthdate: 19700329	**Academic title:** Docent
Gender: Male	**Employer:** Kungliga Tekniska högskolan

Research education

Dissertation title (swe)

Dissertation title (en)

Real Time Motion and Stereo Cues for Active Visual Observers

Organisation	Unit	Supervisor
Kungliga Tekniska Högskolan, Sweden Sweden - Higher education Institutes	CVAP, Datorseende och robotik	Jan-Olof Eklundh

Subject doctors degree	ISSN/ISBN-number	Date doctoral exam
10207. Datorseende och robotik (autonoma system)	0348-2952/91-7283-310-6	2002-06-14

CV

Name: Ahmed Hemani	**Doctorial degree:** 1993-04-05
Birthdate: 19610308	**Academic title:** Professor
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Research education

Dissertation title (swe)

Self-organisation based Scheduling and Binding for High-Level Synthesis of Synchronous Digital Systems

Dissertation title (en)

Self-organisation based Scheduling and Binding for High-Level Synthesis of Synchronous Digital Systems

Organisation	Unit	Supervisor
Kungliga Tekniska Högskolan, Sweden Sweden - Higher education Institutes	Avdelningen för Elektronik och inbyggda system	Gösta Hellgren

Subject doctors degree	ISSN/ISBN-number	Date doctoral exam
10206. Datorteknik	00000-0000	1993-04-05

Publications

Name: Mårten Björkman	**Doctorial degree:** 2002-06-14
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Gender: Male	**Employer:** Kungliga Tekniska högskolan

Björkman, Mårten has not added any publications to the application.

Publications

Name: Ahmed Hemani	**Doctorial degree:** 1993-04-05
Birthdate: 19610308	**Academic title:** Professor
Gender: Male	**Employer:** Kungliga Tekniska högskolan

Hemani, Ahmed has not added any publications to the application.

Register

Terms and conditions

The application must be signed by the applicant as well as the authorised representative of the administrating organisation. The representative is normally the department head of the institution where the research is to be conducted, but may in some instances be e.g. the vice-chancellor. This is specified in the call for proposals.

The signature*from the applicant*confirms that:

- the information in the application is correct and according to the instructions form the Swedish Research Council
- any additional professional activities or commercial ties have been reported to the administrating organisation, and that no conflicts have arisen that would conflict with good research practice
- that the necessary permits and approvals are in place at the start of the project e.g. regarding ethical review.

The signature *from the administrating organisation* confirms that:

- the research, employment and equipment indicated will be accommodated in the institution during the time, and to the extent, described in the application
- the institution approves the cost-estimate in the application
- the research is conducted according to Swedish legislation.

The above-mentioned points must have been discussed between the parties before the representative of the administrating organisation approves and signs the application.

Project out lines are not signed by the administrating organisation. The administrating organisation only sign the application if the project outline is accepted for step two.

Applications with an organisation as applicant is automatically signed when the application is registered.