Application

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Information about applicant

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Information about application

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Subject area:

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Funds applied for

Year:	2016	2017	2018	2019
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Descriptive data

Project info

Project title (Swedish)*

Dataomvandling i tidsdomän

Project title (English)*

Data conversion in time-domain

Abstract (English)*

We aim at finding methods and principles of designing analog-to-digital and time-to-digital converters in deep-submicron technologies. The focus is on developing time-domain signal processing implemented with only switches to maximize the advantage of available fast and inaccurate components. Time-domain processing utilizes parameters like delay, frequency, and phase instead of traditional voltage or current for signal representation. Our goal is to attain converters that have much shorter design time, are portable across different technologies, and are well adapted to support and being supported by digital signal processing hardware. Application area is low-power wireless communication systems. Test chips will be manufactured to show the feasibility of developed theory, proposed models and methods through measurement. Target performance is same as the state of conventional analog design. A major benefit of the proposed approach is that most future technologies, including beyond currently planned CMOS technology nodes, will be able to accommodate high performance converters in close proximity to the vast digital signal processing being offered. Time-domain converters are further expected to have improved time resolution as the technology scales down, while becoming more area and power efficient. This is in contrast with conventional analog design that relies on high-accuracy components unavailable in small scale. In all, we find all-digital time-domain data converter architectures to be very promising for future signal processing.

Popular scientific description (Swedish)*

Dataomvandlare är nödvändiga byggstenar i nästan all elektronik. De används för att översätta signaler som ljud, ljus och radio till digitala signaler som kan behandlas av datorer. I detta projekt forskar vi på nya typer av omvandlare som kan uppnå mycket höga prestanda utan att komponenter med hög precision krävs. Det låga kravet på precision gör att konverterarna blir fördelaktiga att använda i de senaste datorkretsarna och annan elektronik eftersom dessa konstrueras med materialskikt som närmar sig några få atomlagers tjocklek. Då skikt inte går att plana ut under atomnivå så går det inte heller att konstruera komponenter med högre precision än jämnheten på en atomyta. Med dagens teknik går det dessutom inte att tillverka elektroniken så att komponenterna används effektivt om man inte begränsar deras storlek, vilket också begränsar precisionen. För att lösa detta problem så tänker vi undvika konventionell databehandling som arbetar med strömmar och spänningar och istället använda oss av tidspulser i omvandlingen. Fördelen med detta är att komponenterna endast behöver klara av digitala operationer som att slå av och på strömmar, vilket kräver avsevärt lägre precision. På köpet får man dessutom bra prestanda då tidsupplösningen är mycket god i teknologier med de små avstånd som vi är intresserade av. Vårt mål med projektet är därför att finna metoder som möjliggör att de kretsar som är svårast att bygga ska kunna ingå i den elektronik som vi alla kommer att använda i framtiden.

Project period

Number of project years*

4

Calculated project time*

2016-01-01 - 2019-12-31

Classifications

Select a minimum of one and a maximum of three SCB-codes in order of priority.

Select the SCB-code in three levels and then click the lower plus-button to save your selection.

SCB-codes*

2. Teknik > 202. Elektroteknik och elektronik > 20205. Signalbehandling

2. Teknik > 202. Elektroteknik och elektronik > 20204. Telekommunikation

2. Teknik > 202. Elektroteknik och elektronik > 20299. Annan elektroteknik och elektronik

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Enter a minimum of three, and up to five, short keywords that describe your project.

Keyword 1*

all-digital

Keyword 2*

signal processing

Keyword 3*

time-domain

Keyword 4

analog-to-digital conversion

Keyword 5

time-to-digital conversion

Research plan

Ethical considerations

Specify any ethical issues that the project (or equivalent) raises, and describe how they will be addressed in your research. Also indicate the specific considerations that might be relevant to your application.

Reporting of ethical considerations*

The increased efficiency of proposed signal processing will extend the possibilities of information technology, which may be exploited for malicious purposes. The potential harm is however indirect and of general nature, which we believe is more efficiently handled outside a small project like this. Manufacturing of integrated circuits and printed circuit boards involves many chemical substances that are toxic to the environment. Their disposal must be treated responsibly.

The project includes handling of personal data

No

The project includes animal experiments

No

Account of experiments on humans

No

Research plan

Data conversion in time-domain

1 Purpose and aims

Crosstechnology porting of analog intensive data converters is difficult, expensive, and time consuming in deep-submicron CMOS technologies. The high accuracy of the components required in conventional converter architectures is increasingly more difficult to attain due to reduced voltage headroom, reduced intrinsic gain, high levels of noise coupling and a variety of similar reasons [1-4]. Digital components do on the other hand benefit from technology scaling, becoming smaller, faster and more power efficient, and enable improved time resolution. Hence a promising alternative approach to build data converters in future CMOS processes is to use time parameters like delay, frequency, phase etc. for signal representation instead of voltage or current. Resulting signal processing is called time-domain or time-mode signal processing [5, 6]. A time-domain circuit is expected to improve its performance as the technology evolves besides becoming more area and power efficient. Resulting signal processing systems can be implemented with digital circuits, using synthesis and place-and-route of an available digital design flow, which enables better design space exploration compared to a typical full-custom mixed-signal design flow. Hence, it is beneficial to consider time-domain data converter architectures to achieve high performance in deep-submicron CMOS.

A major opportunity in designing time-domain circuits is the possibility to select an architecture with the transistor acting as a switch, turning current on and off, which is an operation that requires significantly less accuracy than obtaining the linear control used in analog circuits. Use of switches and hence large signal swing makes the digital circuits less sensitive to noise than the analog, which is a major obstacle to manage also for digital due to large complexity and small distances between components and connections. Hence it is likely that switches will be preferred in implementation of future signal processing.

This project aims at finding methods and principles of designing data converters in deep-submicron technologies, employing mainly digital switch transistors. Our goal is to advance the performance of time-domain data converters to be on par with traditional analog-intensive, while being synthesizable in digital design flows and implementable in deep-submicron processes. Digital design in modern CMOS processes is already difficult due to large process variability, and many of the conventional analog solutions are almost inconceivable if we are going to exploit the scaling.

Intended application area is low-power and high-performance converters for wireless communications and similar, where we are focusing on analog-to-digital (ADC) and time-to-digital converters (TDC). We hope to achieve ADCs and TDCs that are on par with state-of-the-art analog-intensive techniques. Test chips are designed in deep-submicron CMOS that can be used to validate suggested models, methods and techniques through measurement.

The project is carried out with expertise in switching circuits and substrate noise provided by the principal investigator, Prof. Mark Vesterbacka, active in the Division of Integrated Circuits and Systems, Department of Electrical Engineering, Linköping University, Sweden.

2 Survey of the field

Low-power, high-performance analog-to-digital converters (ADCs) with signal bandwidths up to 20 MHz are of interest in wireless communication. Several all-digital ADCs have been reported recently, targeting such a specification [7-9]. An ADC based on a voltage controlled oscillator (VCO) was demonstrated as early as in 1997 [10], using 1.2 µm CMOS, even though the relative benefits of the technique compared to conventional architectures are not prominent at this technology node. In a time-domain ADC, the input signal is first converted into a time-represented signal like delay, frequency or phase that varies as a function of time. The resulting signal is sampled and quantized to generate corresponding digital codes. An architecture that we have

recently investigated is the VCO-based ADC, discussed in next subsection, which utilizes a VCO to achieve voltage-to-frequency conversion of the input signal. An interesting architecture within this area is the use of a VCO-based quantizer as a part of conventional delta-sigma ADC, achieving high resolution [11-13]. The possibility of using phase as the output of a VCO-based quantizer, instead of frequency, is explored in [13]. An analog delta-sigma pre-modulator is used in front of a VCO-based ADC in [14] to mitigate the problem of VCO non-linearity. Attempts to surpass the time resolution limited by gate delay are made in [15] and in [16] using active and passive phase interpolations respectively. The designs in [17] and [18] are mostly digital, while using custom circuits in ring oscillator delay cells for improved VCO performance. Work [14] improves linearity by introducing a preprocessing stage performing self-oscillating PWM conversion. Other main architectures of interest employ a time-to-digital converter (TDC) to convert the time information into high-resolution digital [19-21], where [20] also introduces a gated VCO, and [21] combine the TDC with a time amplifier. Other recent extensions to the all-digital field are a digital-to-RF converter [22] and an analog amplifier constructed with mainly digital components [23].

2.1 Operation of all-digital ADCs

Figure 1 shows a basic VCO-based ADC (a), which is the predominant architecture of all-digital ADCs. Such converters can be implemented entirely using digital circuits and can even be potentially synthesized from an HDL description. The frequency of the VCO, measured during the sampling intervals defined by a clock signal, provides an estimate of the input signal (b). The counter counts the rising or falling edges, or both, occurring at the output of an ideal (linear) square wave VCO. Counter output is sampled and the first order difference of the resulting sequence constitutes the ADC output (c). Two's complement arithmetic in the counter and the subtractor permits modulo-2^n operation of the counter, provided the counter does not go more than a full cycle within a sampling interval. Besides being scaling friendly and synthesizable, the ADC has several attractive properties like first order noise-shaping and inherent anti-aliasing filtering. The operation principles are similar to those of a conventional first order $\sum\Delta$ ADC, while using frequency for signal representation. It inherits most of the benefits of $\sum\Delta$ ADCs, while avoiding analog components in its structure, making it simple to design and implement. VCO-based ADCs use inherent phase quantization of the VCO to quantize the input signal. Using an N_ϕ stage multi-phase ring oscillator as the VCO, one VCO cycle results in $2N_\phi$ transitions at the output including rising and falling edges, resulting in a phase quantization step size of π/N_ϕ radians. One possible way to implement the ADC involves continuous-time accumulation of the quantized VCO phase followed by a discrete-time differentiation using sampling clock, as shown in the example of Figure 1 (a), yielding samples that are proportional to the average frequency of the VCO.

A model of the VCO-based ADC is shown in Figure 2. The quantized phase $\phi_q(t)$ of the ring oscillator is modeled using a quantizer operating on the continuous phase $\phi(t)$ of the oscillator. $\phi_q(t)$ is then sampled at rate F_s (=$1/T_s$) yielding $\phi_q(kT_s)$. Discrete-time first-order differentiation on $\phi_q(kT_s)$ yields $y(k)$. Figure 3 illustrates the progression of $\phi(t)$ and $\phi_q(t)$ of the VCO. The unquantized phase of the VCO at the end of k^{th} sampling interval, $\phi(kT_s)$ is

$$\phi\left(kT_s\right) = \int_0^{kT_s} \psi\left(v\left(t\right)\right)dt \tag{1}$$

where $\psi(v(t)) = 2\pi(f_0+K_{\text{osc}}v(t))$ describes the voltage-frequency relationship of an ideal VCO. Phase quantization error at the end of the k^{th} sampling interval is $\phi_\varepsilon(kT_s) = \phi(kT_s)–\phi_q(kT_s)$. The output of the ADC can be expressed as

$$y\left(k\right) = \frac{N_\phi}{\pi}\left[\phi_q\left(kT_s\right) - \phi_q\left(\left(k-1\right)T_s\right)\right] = \frac{N_\phi}{\pi}\left[\Delta\phi\left(kT_s\right) - \Delta\phi_\varepsilon\left(kT_s\right)\right] \tag{2}$$

where Δ is the discrete-time backward difference operation $\Delta x(n) = x(n)–x(n–1)$.

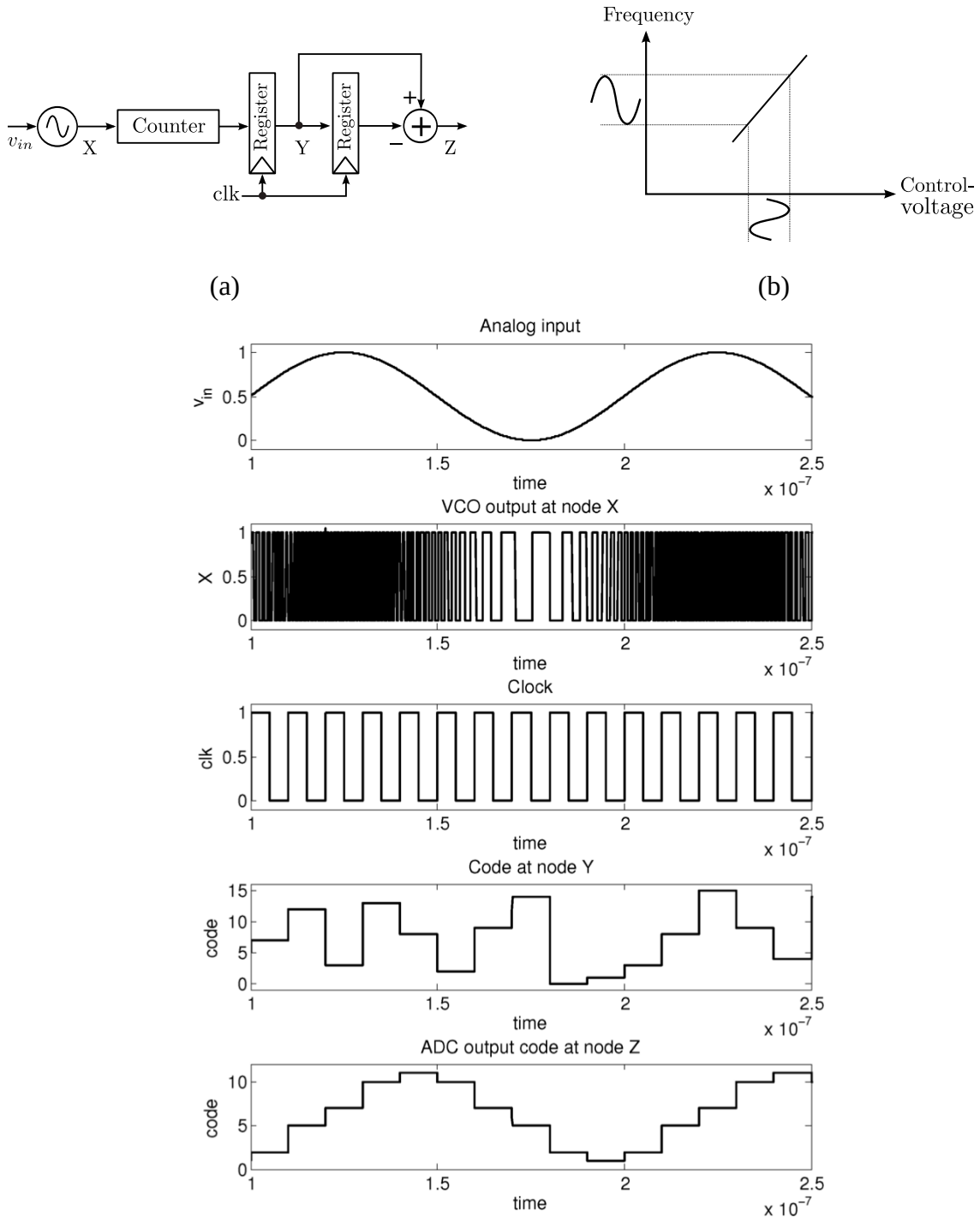

Figure 1. (a) Basic VCO-based ADC with (b) voltage-frequency characteristics, and (c) illustration of the signal processing occurring in the different nodes.

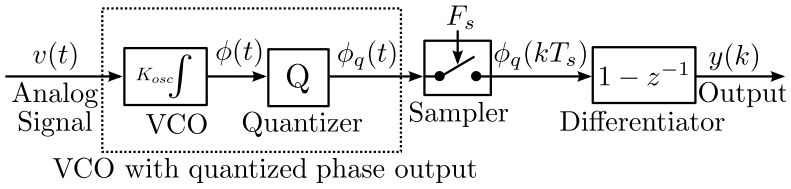

Figure 2. Model of a VCO-based ADC.

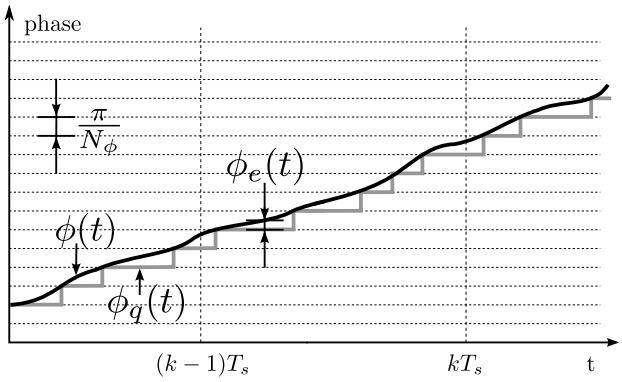

Figure 3. Progression of $\phi(t)$ and $\phi_q(t)$ of the VCO.

Equation (2) becomes

$$Y(s) = \frac{N_\phi}{\pi}\left(1 - z^{-1}\right)\left[\frac{\Psi(s)}{s} - \Phi_\varepsilon(s)\right] \tag{3}$$

in frequency domain, where $z = e^{sT_s}$. The noise transfer function (NTF) and the signal transfer function (STF) are obtained as

$$\text{NTF} = \left.\frac{Y(s)}{\Phi_\varepsilon(s)}\right|_{\Psi(s)=0} = -\frac{N_\phi}{\pi}\left(1 - z^{-1}\right) \tag{4}$$

$$\text{STF} = \left.\frac{Y(s)}{\Psi(s)}\right|_{\Phi_\varepsilon(s)=0} = \frac{N_\phi}{\pi}\left(1 - z^{-1}\right)\frac{1}{s} \tag{5}$$

From (4) it can be seen that the phase quantization noise is first-order shaped. Noise shaping results from the memory of the VCO, which stores and subtracts the residual phase quantization error of one sampling interval from the next. The noise shaping may be exploited by operating the ADC in oversampled mode followed by decimation filtering, improving the resolution over Nyquist mode operation. Another important property hinted by (5) is that the post-quantization periodic continuous-time sampling involves signal integration within sampling intervals, resulting in inherent low pass filtering of the input. Applying (1) in (2) and setting the input to a sinusoid $v(t) = A_{in}\cos(\omega_{in}t)$, we obtain

$$y(k) = C + K_{ADC}A_{in}\cos\left(\frac{\omega_{in}T_s}{2}(2k-1)\right) - E_q \tag{6}$$

where $C = 2N\phi f_0 T_s$ represents the DC component at the output, and

$$K_{ADC} = 2N_\phi K_{osc} T_s \,\text{sinc}\left(\frac{T_s\omega_{in}}{2\pi}\right) \tag{7}$$

represents the ADC gain component where $\text{sinc}(x) = \sin(\pi x)/(\pi x)$, $A_{in}\cos((\omega_{in}T_s/2)(k-1))$ term represents the signal component at the output and $E_q = (N_\phi/\pi)\Delta\phi_\varepsilon(kT_s)$ represents the first-order shaped quantization noise component. Equation (7) shows that the ADC performs a sinc filtering of the input, which relaxes the anti-alias filter design.

2.2 ADC non-idealities

Some of the ADC non-idealities and issues are briefly outlined below. A more detailed discussion is provided in [17].

1) *Non-linearity*: The distortion terms resulting from VCO non-linearity are filtered by the sinc filter described by (7) before getting folded by sampling.

2) *VCO phase noise*: VCO phase noise observed at the phase taps of the ring VCO can be modeled as a noise added to the phase signal, similar to the phase quantization error. Hence, like quantization error, VCO phase noise is also first-order shaped by the ADC.

3) *Mismatch of the delay cells*: The mismatch among delay stages in the ring VCO results in a deterministic error in the phase which can also be modeled as an error added to the phase signal, that also becomes first order-shaped by the ADC.

4) *Clock jitter*: For a given amount of clock jitter, higher VCO frequencies result in larger errors, leading to a signal level dependent sensitivity to jitter. Hence it is beneficial to limit the VCO frequency if jitter estimate is known, such that jitter induced errors shall not dominate the noise sources in the ADC.

5) *Partial sampling*: In contrast to traditional ADCs, the input is first digitized in amplitude and then quantized in time. However, since the time quantization is performed on a digital word, partial sampling errors due to metastability and rise and fall time asymmetry needs to be addressed.

Note that for real all-digital VCO designs, the voltage-frequency conversion characteristics are far from linear as was illustrated in Figure 1 (b). Digital post correction is a necessity, but in our early experiment a scheme based on characterization of the ADC and fitting a static polynomial to an average dynamic condition proved to work surprisingly well. This topic remains to be further investigated.

2.3 Switching noise

Increasing the amount of digital logic often has the side effect of an increased *di/dt* of the supply current, which causes analog circuits and oscillators to experience more problems from power-ground noise [24–27]. Reason for the noise is that digital switching causes a voltage fluctuation on the digital supply rails due to the inductance, resistance, decoupling capacitance and switched capacitance within the package, and the inductance and resistance of the power supply lines, including pin, bond wire, and PCB trace parasitics. This disturbance triggers voltage oscillations on the power lines as can be seen in Figure 4 where noise measurements on a test chip are shown [27]. On the chip we have a digital filter that generates switching noise, and two analog filters that are affected by it. In the left plot we observe the potential of a digital guard used to provide low impedance from the digital ground to the digital circuits, useful for preventing latch up by reducing noise. The initial peak is larger than 50 mV and is followed by a damped oscillation. The noise is cyclostationary in nature, with its characteristics varying periodically with time [28]. Although the substrate used in this chip is lightly p-doped, yielding high impedance, measurements on the bottom plate available in the middle graph shows that most of the noise has propagated through the substrate. Finally it can is seen in the right graph that there is a significant disturbance in the output of one of the analog filters. Clearly we need to use more efficient methods to prevent problems with noise to obtain good performance.

General techniques to combat the noise can be to add more on-chip bypass capacitors, many strategically placed power supply bond wires or use a special package. There are also a number of special circuits and data encoding schemes that reduce the *di/dt*. Our own work in this area includes a circuit technique that reduces the supply noise by shaping its frequency content, and a supply noise filter for digital oscillators [29].

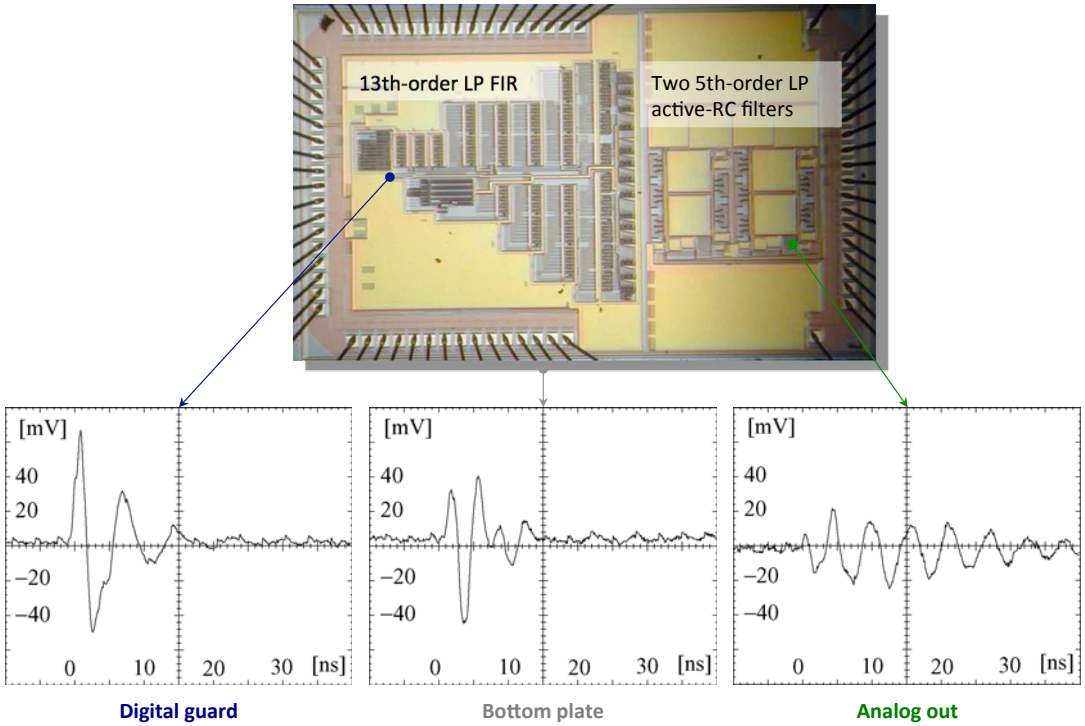

Figure 4. Test circuit with digital and analog filters implemented on substrate with high impedance. The digital filter generates simultaneous switching noise, transferred via substrate and bottom plate to the analog filters as shown by the measurements.

2.4 Digital oscillators

On-chip oscillators are generally sensitive to supply noise, and active oscillators like ring oscillators are especially sensitive [30, 31]. In this project we are interested in exploring coupled oscillator architectures [32–35] and other special circuits that recently have been shown to improve the sensitivity to supply noise [36–38]. Cyclic coupled ring oscillators have traditionally been used to increase the frequency by oscillator pushing, or to implement frequency multiplication. Our objective is to use them for reducing phase noise or increasing the accuracy after combining the phase outputs. A cyclic coupled architecture is depicted for a set of ring oscillators in Figure 5. For a set of *M* ring oscillators (bold drawing), *N* weaker coupling paths are provided (fine drawing). This architecture is shown to improve the resulting phase noise with *M* times over a single oscillator [38]. Another option may be to improve the phase noise by using the structure to increase the frequency, and then divide the phase output(s) to wanted frequency.

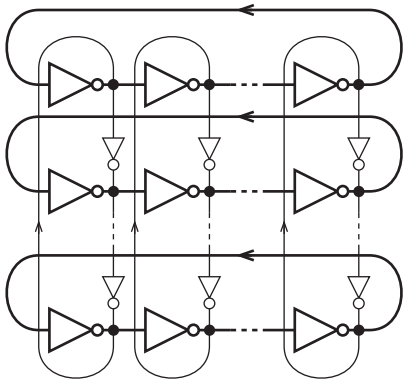

Figure 5. Cyclic coupled ring oscillator.

3 Project description

In this project we aim at finding methods and principles of designing data converters in deep submicron technologies, where the focus is on new time-domain and switch-only techniques to take advantage of future technologies with fast, inaccurate switch components. Main activities follow below.

- Study and improve the sampling technique (occurs in reverse order compared with traditional)
- Investigate differential all-digital ADC architectures
- Improve latency and resolution of our Vernier TDC architecture (investigate time amplification, cyclic, gated and ungated architectures)
- Study cyclic coupled oscillators to improve phase noise and resolution (voltage control schemes are needed)
- Investigate digital dynamic linearity post correction
- Explore design parameter tradeoff (full tradeoff unknown since field is relatively new)
- Maximize design space exploration by designing ADC architectures that can be synthesized in traditional digital design flows

Intended application area is low-power, high-performance ADCs suitable for wireless communications and similar applications. We aim to achieve ADCs that are on par with state-of-the-art analog-intensive techniques. Test chips are designed in deep-submicron CMOS technologies that can be used to validate suggested models, methods and techniques through measurement. A time plan for the project is outlined in Figure 6.

The project starts with a theoretical study and modeling of the reversed order of sampling in VCO-based ADCs. A chip that tests the findings is designed and measured. Next, cyclic coupled oscillators are investigated and modeled, with attention to voltage control. A chip is designed and measured. VCO linearization is studied with subsequent experiment and measurement. Our TDC architecture is improved, designed, and measured. A combination of the findings are collected into a final chip where a differential ADC is designed, which appears to be a promising way to improve performance. Finally digital post correction is studied and applied to previous measurement data. We will disseminate results successively at conferences and in international journals.

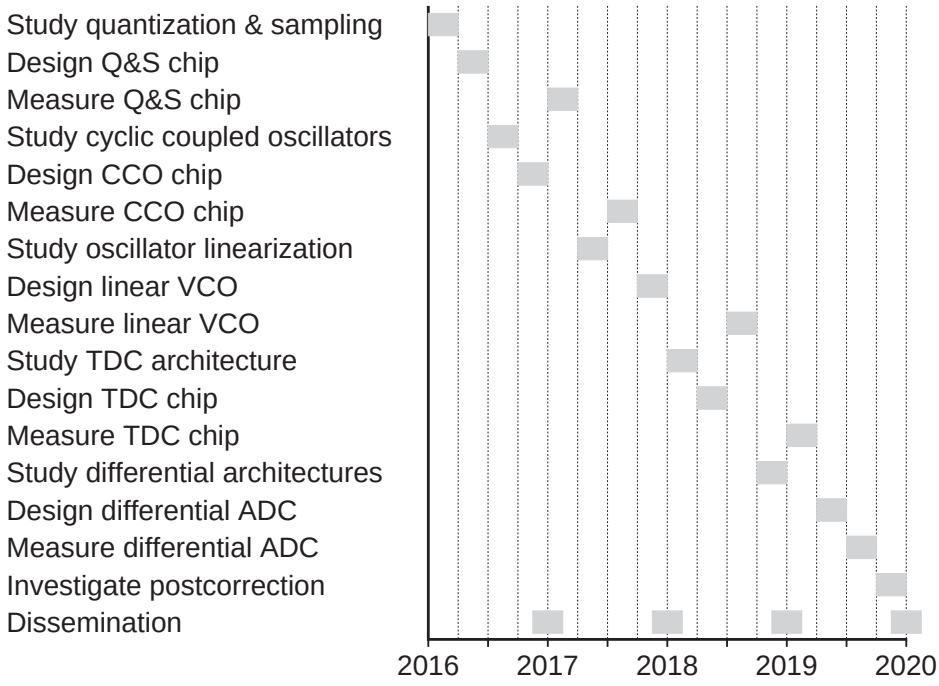

Figure 6. Project time plan.

4 Significance

Previous work has already given us new principles, methods, and architectures for reducing substrate noise as well as achieving a digital ADC and a high performance TDC designed using switch transistors only. This project aims at exploiting the previous work to fully synthesize ADCs and TDCs, and improve their resolution and power performance such that they are competitive with those of conventional state-of-the-art converters. The benefit of this approach is that most future technologies, including *beyond* currently planned CMOS technology nodes since any technology is likely to contain switch components, will be able to accommodate high performance converters in close proximity to the vast digital signal processing hardware being offered. Target figure-of-merit is same as the state of conventional analog design. Theory and methods we suggest will be validated by measurements on actual implementations showing the feasibility of our proposals.

5 Preliminary results

We have recently designed a VCO-based ADC and a new TDC architecture where we have started to address some of the issues in this application.

5.1 VCO-based ADC

In a recent experiment we aimed for an all-digital VCO-based ADC design, which uses standard digital circuits in contrast to some of the recently published works that employ custom designed analog delay cells in the VCO. Major inventions is a technique that limits the instantaneous error resulting from metastability and sampling of digital data to one LSB, and a new digital post correction method. The design was fabricated in a commercial 65 nm digital CMOS technology and the measured results are available in Figure 7 (a) along with a comparison with state-of-the-art. Our design has competitive performance and uses only switch transistors. Table is taken from our recent article [39].

5.2 Vernier TDC

We have proposed a TDC Vernier-chain architecture based on a new type of delay latch that saves power. This architecture performs well and we would like to investigate some ideas on how to improve and use it in this project. Measured data from a test chip is presented and compared with state-of-the art in Figure 7 (b) [40].

Performance metric	[14]	[17]	[13]	[12]	This work
Sampling (MHz)	300	500	600	640	205
OSR	5	25	15	16	4
Bandwidth (MHz)	30	10	20.0	20.0	25.62
ENOB	8.3	9[a]	8.43[a]	7.35[a]	8.1
SNDR (dB)	52	56[b]	52.5	46	50.3
SNR (dB)	-	63.1	55.1	46.2	52.8
SFDR (dB)	54	72	64.0	67	55.3
Power (mW)	5.7	12.6	14.3	6.3[c]	3.3
FoM (fJ/step)	294	1010	1040[d]	960[d]	235
Area (mm^2)	0.009	0.078	0.12	0.026	0.026
Synthesizable[e]	-	-	-	-	Yes
Technology (nm)	65	130	130	90	65

(a)

Type	[14] Passive interp.	[15] Cyclic Vernier	[16] 2-D delay line	[17] Vernier + GRO	This Work
Samp. rate [MS/s]	180	10	50	25/100	100
Resolution [ps]		5.5	4.8	5.8	5.7
Oversampling ratio	4			16	
Res. w. interp. [ps]	4.7			3.2	
Power supply [V]	1.2	1.0	1.2	1.2	1.2
Power [mW]	3.6	2.0	1.7[a]	3.6[b]	1.14/1.75[c]
Range [ns]	0.6	100	0.6	40	0.73
Number of bits	7	15	7		7
Area [mm^2]	0.02	0.006	0.02	0.027	0.004
Technology [nm]	90		65	90	65
Year	2008	2011	2010	2012	2014

(b)

Figure 7. Comparison of recent (a) VCO-based ADCs, and (b) TDCs with our work.

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Interdisciplinarity

My application is interdisciplinary

☐

An interdisciplinary research project is defined in this call for proposals as a project that can not be completed without knowledge, methods, terminology, data and researchers from more than one of the Swedish Research Councils subject areas; Medicine and health, Natural and engineering sciences, Humanities and social sciences and Educational sciences. If your research project is interdisciplinary according to this definition, you indicate and explain this here.

Click here for more information

Scientific report

Scientific report/Account for scientific activities of previous project

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Budget and research resources

Project staff

Describe the staff that will be working in the project and the salary that is applied for in the project budget. Enter the full amount, not in thousands SEK.

Participating researchers that accept an invitation to participate in the application will be displayed automatically under Dedicated time for this project. Note that it will take a few minutes before the information is updated, and that it might be necessary for the project leader to close and reopen the form.

Dedicated time for this project

	Role in the project	Name	Percent of full time
1	Applicant	Mark Vesterbacka	40
2	Participating researcher	Ny doktorand	80

Salaries including social fees

	Role in the project	Name	Percent of salary	2016	2017	2018	2019	Total
1	Applicant	Mark Vesterbacka	40	450,000	450,000	450,000	450,000	1,800,000
2	Participating researcher	Ny doktorand	80	450,000	450,000	450,000	450,000	1,800,000
	Total			900,000	900,000	900,000	900,000	3,600,000

Other costs

Describe the other project costs for which you apply from the Swedish Research Council. Enter the full amount, not in thousands SEK.

Premises

	Type of premises	2016	2017	2018	2019

Running Costs

	Running Cost	Description	2016	2017	2018	2019	Total
1	Test circuits	Chip and PCB manufacturing 40 nm CMOS MPW	150,000	150,000	150,000	150,000	600,000
2	Dissemination costs	Journal publication and conference travel	50,000	50,000	50,000	50,000	200,000
3	IT	Computers, software, phone	50,000	50,000	50,000	50,000	200,000
	Total		250,000	250,000	250,000	250,000	1,000,000

Depreciation costs

	Depreciation cost	Description	2016	2017	2018	2019

Total project cost

Below you can see a summary of the costs in your budget, which are the costs that you apply for from the Swedish Research Council. Indirect costs are entered separately into the table.

Under Other costs you can enter which costs, aside from the ones you apply for from the Swedish Research Council, that the project includes. Add the full amounts, not in thousands of SEK.

The subtotal plus indirect costs are the total per year that you apply for.

Total budget

Specified costs	2016	2017	2018	2019	Total, applied	Other costs	Total cost
Salaries including social fees	900,000	900,000	900,000	900,000	3,600,000		3,600,000
Running costs	250,000	250,000	250,000	250,000	1,000,000		1,000,000
Depreciation costs					0		0
Premises					0		0
Subtotal	1,150,000	1,150,000	1,150,000	1,150,000	4,600,000	0	4,600,000
Indirect costs	400,000	400,000	400,000	400,000	1,600,000		1,600,000
Total project cost	1,550,000	1,550,000	1,550,000	1,550,000	6,200,000	0	6,200,000

Explanation of the proposed budget

Briefly justify each proposed cost in the stated budget.

Explanation of the proposed budget*

Salary 1) The professor will contribute with 20% supervision and 20% research to the project.
Salary 2) The new PhD student will have this project as main thesis topic and spend a standard 80% share on research and 20% share on teaching. Cost 1) To publish in the best international journals in our field, it is crucial to design, manufacture, and test silicon chips to show concepts and performance in real experiments.
Cost 2) Dissemination of results is crucial for any scientific work. This is an estimate of the publishing costs in internaional journals and travel and conference fees for the two project participants.
Cost 3) Computers with proper CAD software are essential in this project.

Other funding

Describe your other project funding for the project period (applied for or granted) aside from that which you apply for from the Swedish Research Council. Write the whole sum, not thousands of SEK.

Other funding for this project

Funder	Applicant/project leader	Type of grant	Reg no or equiv.	2016	2017	2018	2019

CV

CV 2015-03-27 — Mark Vesterbacka

1 Higher education qualification

1991, Civilingenjör i Teknisk fysik och elektroteknik (Y), LIU

2 Doctor degree

1997, Elektroniksystem, LIU, “On Implementation of Maximally Fast Wave Digital Filters”, supervisor L. Wanhammar

3 Postdoctoral positions

4 Qualification required for appointment as a docent

2002

5 Current position

Professor, LIU, 2002–, 30% research

6 Previous positions and periods of appointment

Universitetslektor, LIU, 1998–2002
Temporary universitetslektor, LIU, 1997–1998
Doctoral student, LIU, 1991–1997

7 Interruption in research

Parental leave 12 months 2008–2009

8 Supervision, main doctor supervisor

N.U, Andersson, LIU, 2014
E. Backenius, LIU, 2007
E. Säll, LIU, 2007
M. Karlsson, LIU, 2005
K.O. Andersson, LIU, 2005

9a Visiting scholar

9 months 2009-2010, BWRC, University of California, Berkeley

9b Professional society membership

IEEE, S'91-M'98-SM'06

9c Various commissions

Expert reviewer, program application civ.ing. HH, KK Avans, 2014
Expert reviewer, examination right civ.ing. HIG, Högskoleverket, 2012
Expert reviewer, docent LTU, Sweden, 2011
Expert reviewer, universitetslektor UMU, Sweden, 2011
Expert reviewer, universitetslektor LTU, Sweden, 2007
Expert reviewer, professor LU, Sweden, 2006
Expert reviewer, forskarassistent LTU, Sweden, 2005

Expert reviewer, VR NT-L, 2002–2003
Vice chairman, NORCHIP 2006
TPC chair, EECTD 2011
TPC member, NORCHIP 2006–2014
Session chair, NORCHIP 2006
Session chair, ECCTD 2005
Session chair, RVK 2005
Session chair, SSoCC 2003
Session chair, SSMSD 2003
Session chair, ICECS 2000
Session chair, IAVLSIW 2000
Reviewer, Springer Wireless Personal Comm., 2012–
Reviewer, Springer Analog IC & Signal Proc., 2007–
Reviewer, IEEE Trans. Circ. & Syst. (TCAS)-I , 2004–
Reviewer, IEEE Trans. Circ. & Syst. (TCAS)-II, 2002–
Reviewer, IEEE Trans. VLSI, 2007–
Reviewer, IEEE Signal Proc. Letters, 2003–
Reviewer, IET Proc. Computers & Digital Tech., 2003–
Reviewer, Integration—The VLSI J., 2003–
Reviewer, international conferences
Opponent, doctor, UIO, Norge, 2011
Opponent, doctor, LTU, 2008
Opponent, doctor, MIU, 2007
Opponent, doctor, HUT, Finland, 2006
Opponent, doctor, LTH, 2003
Opponent, doctor, TUT, Finland, 2002
Examination committee, docent LIU, 2014
Examination committee, doctor, LTU, 2014
Examination committee, doctor, LTU, 2012
Examination committee, doctor, LTU, 2010
Examination committee, doctor, LIU, 2010
Examination committee, doctor, KTH, 2008
Examination committee, doctor, LTH, 2008
Examination committee, doctor, MIU, 2008
Examination committee, doctor, LIU, 2007
Examination committee, doctor, CTH, 2007
Examination committee, doctor, KTH, 2006
Examination committee, doctor, LTH, 2005
Examination committee, doctor, LTH, 2004
Examination committee, doctor, LIU, 2004
Examination committee, doctor, KTH, 2005
Examination committee, doctor, LTH, 2004
Examination committee, doctor, LTU, 2004
Examination committee, doctor, KTH, 2003
Examination committee, doctor, LTH, 2003
Examination committee, doctor, KTH, 2003
Examination committee, doctor, LIU, 2002
Preexamination, doctor, VU, Australien, 2003
Preexamination, doctor, TUT, Finland, 2003

Publication list

Publications 2007-2014 — Mark Vesterbacka

Publication data base: Google Scholar

Five most relevant publication for the project is marked with a star *.

Five most cited works

i. M. Vesterbacka, “A 14-Transistor CMOS Full Adder with Full Voltage-Swing Nodes,” in *Proc. IEEE Workshop on Signal Processing Systems*, SiPS’99, Taipei, Taiwan, Oct. 20-22, 1999, pp. 713-722. Citations: 67

ii. M. Vesterbacka: On Implementation of Maximally Fast Wave Digital Filters, Dissertation No. 487, Linköping University, June 1997. Citations: 37

iii. E. Säll and M. Vesterbacka, “A Multiplexer Based Decoder for Flash Analog-to-Digital Converters,” in *Proc. IEEE Analog and Digital Techniques in Electrical Engineering*, TENCON'04, vol. 4, Chiang Mai, Thailand, Nov. 21-24, 2004, pp. 250-253. Citations: 34

iv. E. Säll, M. Vesterbacka, and K.O. Andersson, “A Study of Digital Decoders in Flash Analog-to-Digital Converters,” in *Proc. IEEE Int. Symp. Circuits and Systems*, ISCAS’04, vol. 1, Vancouver, Canada, May 2004, pp. 129-132. Citations: 33

v. E. Säll and M. Vesterbacka, “Thermometer-to-Binary Decoders for Flash Analog-to-Digital Converters,” in *Proc. European Conf. Circuit Theory and Design*, ECCTD’07, Sevilla, Spain, Aug. 26-30, 2007, pp. 240-243. Citations: 25

1 Peer-reviewed original articles

*[1] V. Unnikrishnan and M. Vesterbacka, “Time-Mode Analog-to-Digital Conversion Using Standard Cells,” *IEEE Trans. Circuits Syst. Part I: Regular Papers*, vol. 61, no. 12, pp. 3348-3357, Dec. 2014.

*[2] N.U. Andersson and M. Vesterbacka, “A Vernier Time-to-Digital Converter With Delay Latch Chain Architecture,” *IEEE Trans. Circuits Syst. Part II: Express Briefs*, vol. 61, no. 10, pp. 773-777, Oct. 2014. Citations: 1

[3] S. Asif and M. Vesterbacka, “Performance Analysis of Radix-4 Adders,” *Elsevier Integration, the VLSI Journal*, vol. 45, no. 2, pp. 111-228, March 2012.

*[4] S.M.Y. Sherazi, S. Asif, E. Backenius, and M. Vesterbacka, “Reduction of Substrate Noise in Sub Clock Frequency Range,” *IEEE Trans. Circuits Syst. Part I: Regular Papers*, vol. 52, no. 11, pp. 1287-1297, June 2010. Citations: 4

2 Peer-reviewed conference contributions

*[5] M.T. Pasha and M. Vesterbacka, “A Modified Switching Scheme for Multiplexer Based Thermometer-to-Binary Encoders,” in *Proc. Nordic Event in ASIC Design Conf.*, NORCHIP’14, Tampere, Finland, Oct. 27-28, 2014.

[6] V.S. Sadeghi, S.I. Saeed, S. Calnan, M.P. Kennedy, H.M. Naimi, and M. Vesterbacka, “Simulation and Experimental Investigation of a Nonlinear Mechanism for Spur Generation in a Fractional-N Frequency Synthesizer,” in *Proc. IET Irish Signals and Systems Conference,* ISSC’12, Maynooth, Ireland, June 28-29, 2012.

*[7] M.T. Pasha and M. Vesterbacka, “Frequency Control Schemes for Single-Ended Ring Oscillators,” in *Proc. European Conf. Circuit Theory and Design*, ECCTD’11, Linköping, Sweden, Aug. 29-31, 2011, pp. 361-364.

[8] A. Jalili, S.M. Sayedi, J.J. Wikner, N.U. Andersson, and M. Vesterbacka, “Calibration of ΣΔ Analog-to-Digital Converters Based on Histogram Test Methods,” in *Proc. Nordic Event in ASIC Design Conf.*, NORCHIP’10, Copenhagen, Denmark, Nov. 12-13, 2010, pp. 1-4. Citations: 2

[9] A. Jalili, S.M. Sayedi, J.J. Wikner, K. Palmkvist, and M. Vesterbacka, “Calibration of High-Resolution Flash ADCs Based on Histogram Test Methods,” in *Proc. IEEE Int. Conf. Elec., Circ. Syst.*, ICECS’10, Athens, Greece, Dec. 12-15, 2010, pp. 114-117.

[10] J. Castro, A.J. Acosta, and M. Vesterbacka, “Geometry Optimization in Basic CMOS Cells for Improved Power, Leakage, and Noise Performances,” in *Proc. Int. Conf. on Advances in Electronics and Microelectronics*, ENICS’08, Sept. 29-Oct. 4, 2008, pp. 48-53. Citations: 1

[11] E. Backenius, M. Vesterbacka, and V.B. Settu, “Reduction of Simultaneous Switching Noise in Analog Signal Band,” in *European Conf. Circuit Theory and Design*, ECCTD’07, Sevilla, Spain, Aug. 2007, pp. 148-151. Citations: 1

[12] E. Säll and M. Vesterbacka, “Thermometer-to-Binary Decoders for Flash Analog-to-Digital Converters,” in *Proc. European Conf. Circuit Theory and Design*, ECCTD’07, Sevilla, Spain, Aug. 26-30, 2007, pp. 240-243. Citations: 25

3 Monographs

4 Research review articles

[13] M. Vesterbacka and J. Madsen, “Editorial: Selected Papers from NORCHIP '06,” *IET Proc. Computers & Digital Techniques*, vol. 2, no. 4, pp. 251-252, 2008.

[14] L. Wanhammar and M. Vesterbacka, “Guest Editorial,” *Springer Analog IC & Signal Proc.*, vol. 54, no. 2, pp. 75-76, 2008.

5 Books and book chapters

6 Patents

7 Open access computer programs

8 Popular science articles/presentations

CV

Name: Mark Vesterbacka	**Doctorial degree:** 1997-06-06
Birthdate: 19660304	**Academic title:** Professor
Gender: Male	**Employer:** Linköpings universitet

Research education

Dissertation title (swe)

Dissertation title (en)

On Implementation of Maximally Fast Wave Digital Filters

Organisation	Unit	Supervisor
Linköpings universitet, Sweden Sweden - Higher education Institutes	Institutionen för systemteknik (ISY)	Lars Wanhammar

Subject doctors degree	ISSN/ISBN-number	Date doctoral exam
20205. Signalbehandling	0345-7524/91-7871-947-X	1997-06-06

Publications

Name: Mark Vesterbacka	**Doctorial degree:** 1997-06-06
Birthdate: 19660304	**Academic title:** Professor
Gender: Male	**Employer:** Linköpings universitet

Vesterbacka, Mark has not added any publications to the application.

Register

Terms and conditions

The application must be signed by the applicant as well as the authorised representative of the administrating organisation. The representative is normally the department head of the institution where the research is to be conducted, but may in some instances be e.g. the vice-chancellor. This is specified in the call for proposals.

The signature*from the applicant*confirms that:

- the information in the application is correct and according to the instructions form the Swedish Research Council
- any additional professional activities or commercial ties have been reported to the administrating organisation, and that no conflicts have arisen that would conflict with good research practice
- that the necessary permits and approvals are in place at the start of the project e.g. regarding ethical review.

The signature *from the administrating organisation* confirms that:

- the research, employment and equipment indicated will be accommodated in the institution during the time, and to the extent, described in the application
- the institution approves the cost-estimate in the application
- the research is conducted according to Swedish legislation.

The above-mentioned points must have been discussed between the parties before the representative of the administrating organisation approves and signs the application.

Project out lines are not signed by the administrating organisation. The administrating organisation only sign the application if the project outline is accepted for step two.

Applications with an organisation as applicant is automatically signed when the application is registered.